ELECTRICAL PROPERTIES OF HIGH RESOLUTION DOPING STRUCTURES

BY

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This thesis is dedicated to;

To my mother,

and my father who never saw the completion of my work.

SUMMARY

The electrical transport properties and device applications of certain high resolution doping structures in silicon are discussed in this thesis. The promise of enhanced device properties from a high resolution doping structure was envisaged through the use of doping superlattices. These structures are unobtainable by typical high temperature silicon processing technology and are well suited to fabrication by Molecular Beam Epitaxy. The potential for enhanced mobilities in Boron and Antimony doping superlattices has been investigated by the author. Interpretation of mobility data proved complex due to the number of parallel conduction paths, however, some apparent mobility enhancement was found. Sample fabrication during this work has evolved from the use of crude in house contacts, to microfabricated structures produced by the Edinburgh Microfabrication Facility. This allowed the use of well-defined sample geometries and ohmic contacts to buried doping spikes.

Conductivity and Hall coefficient studies are continued by a study of Si:Sb layers of widths between 5 to 500nm. A metal-insulator transition is observed as the width of the dopant spike is reduced to 5nm. Further measurements on Si:Sb doping spikes of widths 10,20, 80nm at low temperatures 300mK-25K, have been interpreted through the use of weak localisation and electron-electron interaction corrections to the Boltzmann conductivity. Also obtained through magnetoresistance experiments is the first observation of a 2D to 3D transition in the low temperature electrical properties.

The simplest doping profile available in MBE is believed to be one in which the dopant atoms are confined to a few lattice constants, known as a "Delta" layer. This allows the study of two dimensional phenomena in a homoepitaxial system without the presence of an hetero-interface as in the Si-MOSFET. The two dimensional quantisation of the electric subbands in Boron and Antimony delta layers has been investigated via tunnelling spectroscopy. The resultant spectra were found to be consistent with theoretical calculations of subband structure.

Finally, the device application of a delta layer was investigated through the development of the first p-channel boron delta doped FET, which may offer advantages for submicron VLSI technology.

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DECLARATION

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It contains an account of my own research carried out in the Department of Physics at Portsmouth Polytechnic and the Department of Physics at the University of Warwick during the period October 1985 to August 1992. It is presented according to Department of Physics guidelines, Phys/PG3. The work described in this thesis is the result of my own research, except where specifically acknowledged in the text.

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Biswas R.G., Hopkinson M., Houghton R.F., Smith D.W., Parker E.H.C., Whall T.E., "Synthesis and characterisation of doping superlattices for studies of electrical transport", J.Electrochem. Soc., **88**, 545(1988). Incorporated in Chapter 4.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

In 1980, *Wood* and co-workers reported the first growth of an extremely narrow doping layer in GaAs using the technique of Molecular Beam Epitaxy. The prospect that the thickness of the doping layer might be as small as one atomic layer, has led to the term "delta doping". Dohler (1978) discussed the possibility that thin layer doping structures would provide an important material system for the study of low dimensional transport phenomena. Such doping structures in silicon, allow the study of 2-dimensional effects without the presence of an oxide barrier, as in a MOSFET(metal oxide semiconductor field effect transistor), giving precise control of disorder and an absence of image forces. Classical or wave mechanical spreading of the charge carriers also allow the possibility of enhanced carrier mobilities as compared to uniformly doped material. Delta doping also provides the prospect of new devices such as the Camel transistor [*Shannon* 1979], novel infra red detectors [*Tempel* 1990] and the Delta doped FET [*Schubert & Ploog* 1985a]. This thesis presents work on the electrical characteristics of high resolution doping structures in silicon, and their application to the delta doped FET. Electrical characterisation has been performed by Hall, conductivity measurements, electrochemical capacitance voltage profiling and tunnelling spectroscopy. An investigation has been made of quantum interference scattering mechanisms in electrical conduction at low temperatures on a range of Antimony doped layers, and where a 3D to 2D transition is demonstrated. A periodic sequence of narrow doping spikes, known as a doping superlattice, has been

investigated for enhanced carrier mobilities. Finally, the development and characteristics of a p-channel delta doped FET is reported. This chapter introduces the subject areas under investigation in this work.

1.1.1 SILICON MOLECULAR BEAM EPITAXY

The rapidly maturing technology of silicon molecular beam epitaxy (Si-MBE) [*Kasper & Bean* 1988] has enabled the growth of "designer" semiconductor structures, where matrix composition, spatial resolution and impurity profiles can be carefully controlled. Thus it is now possible to design semiconductor structures not available using current semiconductor processing technology. The continuing trend towards sub-micron very large scale integration (VLSI), with the need for improved device speed and packing density may allow the use of Si-MBE epitaxial layers incorporating novel device designs and doping profiles to be part of a future VLSI silicon chip.

Typically MBE growth occurs in ultra high vacuum conditions of 10^{-11} mbar, with a growth pressure of 10^{-8} mbar and substrate temperatures between 450-850°C. Epitaxial layer growth occurs on atomically clean substrates by way of a two dimensional growth mode [*Allen & Kasper* 1988]. This allows layer growth to be accurately controlled. Electron beam evaporation of silicon allows growth rates of $< 1 nms^{-1}$, combined with co-evaporation doping or low energy implantation to give nanometre control of dopant profiles. Typical dopants include elemental boron and antimony for p and n-type doping respectively. Doping uniformity is typically between 5-10% across a 3inch wafer with n-type background doping of approximately $10^{15}cm^{-3}$. [For a review of current(1991) Si-MBE technology see MRS Si-MBE 1991]. The use of solid phase epitaxy(SPE), can allow dopant planes to be deposited at very low temperature < 500°C, to give diffusional profile smearing over only a few lattice constants. SPE involves recrystallisation of an amorphous cap in which the ultimate

dopant profile of a Dirac delta function distribution of dopants is incorporated. Low temperature growth of boron doped layers, gives full activation, with low profile smearing [*Kubiak et al* 1991]. High substrate temperatures combined with Potential Enhanced Doping(PED) give the best profile control of antimony doped layers.

1.2 DEVICE PROSPECTS

Molecular beam epitaxy has three advantages over conventional processing technology [*Allen* 1985]: (i) totally new devices that could not be fabricated by any other means, (ii) improved dopant profile control, (iii) combination of Si with other semiconductor materials, e.g. Si/SiGe [*Roosevelt* 1986] are possible. Historically the MBE of III-V materials has led the development of new device structures. This has been due in part to the simpler technology of III-V MBE, and in part due to the greater possibilities that exist in producing novel device or improved structures through the use of band gap engineering. An example is given by the two dimensional gas formed in the high electron mobility transistor(HEMT) [*Sakaki* 1986]. Here the lattice mismatch produces a potential well for electrons, in which the spatially separated electrons have very few scattering centres giving a high mobility. The lower effective mass for charge carriers and the availability of semi-insulating substrates has enhanced the development of III-V devices, as compared to silicon. However, because of the greater technological importance of silicon, increasing attention is being given to the production of silicon devices utilising molecular beam epitaxy.

MBE is capable of producing two types of device structures, those where conduction is parallel to the growth direction and the more numerous vertical devices for transport perpendicular to the epitaxial layer. The latter is made possible by the controllability of MBE in the growth direction. Concentrating on homoepitaxy, the devices can be subdivided into demonstration(novel), and improved conventional

devices. For example, a Si-MBE epitaxial layer may be substituted for the conventional CVD (chemical vapor deposition) epitaxial layer used in Bipolar or CMOS (complementary metal oxide semiconductor) circuits [*Sze* 1988]. Advantages include hyperabrupt PN junctions to maximise current gain and speed, and lower autodoping of the epitaxial layer. Improved vertical devices include IMPATT diodes (impact ionisation avalanche transit time), camel diodes, planar doped diodes, and triangular barrier diodes [*Reviewed in Board* 1985, *Wood C.E.C.* 1981]. New transistor structures include the hot electron transistor [*Board* 1985] and the delta doped field effect transistor [*Schubert et al* 1986b]. The latter appears to offer significant advantages in the sub-micron regime and is investigated in the present work.

Band gap engineering utilising heterojunctions has allowed the development of the MODFET (modulation doped field effect transistor), usually offered by GaAlAs/GaAs or Si/SiGe systems. This device has a very high mobility for low electric fields between source and emitter giving rise to a short transit time for the charge carriers. However, in the submicron regime the transit time is dependent on the saturation drift velocity and the number of charge carriers, although a high mobility will minimise parasitic time delays.

Totally new device structures may be fabricated from a sequence of n-i-p-i layers or doping superlattices. This type of doping structure can not be realised with conventional CVD process. Although research in this area has been concentrated in the III-V materials, its potential in silicon has yet to realised.

There are then two approaches to the implementation of Si-MBE into VLSI technology. First, the epitaxial layer may incorporate a novel dopant profile as described earlier or limited area growth on a patterned substrate. The latter could involve limited area epitaxial growth on an insulator as used in SOI (Silicon on insulator) technology. A low temperature MBE layer will reduce thermal stresses and auto doping effects. Ultimately the use of any Si-MBE layer is afforded by its incorporation into current VLSI processing technology. Problem areas remain in the use of a high temperature stage for gettering and implant activation. Thus, future VLSI

incorporation may require low temperature oxidation and rapid thermal anneal treatments.

1.3 PREVIOUS WORK

1.3.1 DELTA DOPING

Ultra thin doped layers have been proposed as two dimensional systems, in which the charge carriers are subject to a strong space charge potential [*Dohler* 1978], allowing the energy subband spectrum to be quantised, similar to that observed in the Si-MOSFETs. The concept of delta doping where the impurity distribution is confined to a monolayer or a few lattice constants, has enabled a 2D distribution of confined carriers to be studied in a homoepitaxial system. Delta doped layers have now been extensively studied in GaAs, with quantum confinement effects demonstrated by Shubnikov-de Hass oscillations [*Gillman et al* 1988], infrared excitation [*Tempel et al* 1990] and tunnelling spectroscopy [*Zachau et al* 1989]. Delta doping of silicon has used boron, gallium and antimony as the dopants [Mattey *et al* 1990, Gorkum 1987]. The extremely narrow widths of boron delta layers produced by the University of Warwick Si:MBE group have proved difficult to measure. Structural analysis by X-ray diffraction gave an upper limit of 2nm [*Powell et al* 1991b], and secondary ion mass spectrometry profiles [*Mattey et al* 1990a] gave the width as <2.7nm(Full width at half maximum). This was also confirmed by a transmission electron microscopy measurement of 2nm. Capacitance voltage measurements showed extremely sharp doping profiles [*Mattey et al* 1990b, *Gorkum et al* 1989, *Schubert et al* 1986a], with the width dependent on the extent of the electron wavefunction. Hall measurements indicated that a smaller mean separation between dopant atoms as compared to the bulk is required to obtain metallic behaviour at low temperatures [*Eisele* 1987, *Mattey et al* 1990a]. Recent work has involved the investigation of the anisotropy of the

magnetoresistance of a 2D distribution of carriers [*Mattey et al* 1992b] in a boron delta layer. The practical applications of a delta doped FET devices are of continuing current interest [*Board* 1992, *Biswas et al* 1992a, *Chen* 1992].

1.4 ELECTRICAL TRANSPORT

1.4.1 TUNNELLING SPECTROSCOPY

Two dimensional effects where electron motion is restricted by the discrete subbands can be found in the Si-MOSFET and GaAlAs/GaAs heterostructures. If a thin doping spike of width equal to the thermal de-Broglie wavelength of carriers in the bulk is placed in a semiconductor, then the space charge potential leads to the formation of a quantum well. The subband structure formed, changes the density of states to a "staircase" function and can be investigated by observing discontinuities in the tunnel current voltage characteristic of a suitable geometry structure.

The basic principle of tunnelling requires that an electron with an incident energy less than the height of a potential barrier has a finite probability of transmission through the barrier. The electron probability density $\psi^*\psi$ (where ψ is the Schrodinger's wavefunction) is a continuous function at the barrier and decays exponentially through the barrier.

Tunnelling spectroscopy has been used extensively to observe the band structure of semiconductor devices. For example p-n junction tunnelling occurs in an Esaki diode, while resonant tunnelling between 2D subbands occurs in double barrier heterostructures [*Capasso et al* 1986]. Tunnelling of electrons(holes) from a 3D to 2D system has been studied in a metal oxide semiconductor system(MOS) by Kunze(1984). The quantisation of a thin doping spike predicted by Dohler(1978) has been investigated in a bipolar tunnelling device by Prechtel *et al* (1984). The electronic subband structure for a Si δ-layer in GaAs was demonstrated by Zachau *et al* (1986), whereby using a

Schottky barrier, electrons could tunnel through a thin cap to 2D subbands. The cap layer thickness was sufficiently narrow (20nm), to allow a measurable tunnelling current. Figure 1.1 shows the potential profile of an n^+ delta layer in a p^- background. For this case, a negative gate bias (V_g) on the metal gate will lower the Fermi level in the metal and allow electrons to tunnel from occupied states in the delta layer. For a positive V_g, the Fermi level sweeps the position of an unoccupied subband, and electrons can tunnel from the well into the metal.

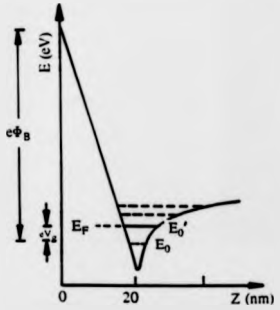


Figure 1.1 Potential profile for an n-type delta layer in a tunnelling spectroscopy experiment. After *Eisele (1989)*.

Since the 2D density of states is a step like function, the differential conductance dI/dV_g will similarly show discontinuities due to the 2D subband structure. Measurement of the tunnelling current requires the cap thickness to be optimised so that the excess tunnelling current does not swamp the contribution of the 2-D subbands. Eisele(1989) used a dimensionless quantity of $(dI/dVg)/(I/V)$ to approximately cancel the exponential tunnelling current. Masking of the subband discontinuity is also

affected by increased background doping [*Eisele* 1989]. Although this should increase the depth of the well and the relative separation of the subbands, the discontinuities in the tunnelling current may be masked by impurity smearing. Experimental data on delta layers in silicon have only given broad agreement between theory and experimental subband structure and is discussed in this work, chapter 4.2 [*Eisele* 1989, *Li et al* 1989, *Biswas et al* 1991].

1.4.2 QUANTUM CORRECTIONS TO THE BOLTZMANN CONDUCTIVITY

The transport properties of low dimensional structures, where electron (hole) transport is restricted in one or more degrees of freedom has been the subject of much experimental work for the last 15 years [*Harris et al* 1989] and includes the quantum Hall effect, resonant tunnelling through double barriers, miniband transport in superlattices and one dimensional ballistic resistance. Most experimental work concerned with thin semiconductor layers has concentrated on the GaAs/AlGaAs material system. In silicon, the n-channel MOSFET has been the most thoroughly investigated system, where a thin inversion layer(10nm) of electrons is formed by a positive gate potential. The Fermi level may be varied by the gate bias to give electron concentrations of up to $10^{13}cm^{-2}$. Channel implants during fabrication can vary the characteristic scattering times and hence the carrier mobility. Parallel transport in the layer is determined by the subband structure, which for a Si-MOSFET usually involves one or two subbands. Static disorder is introduced by the SiO_2 interface. Measurements of the resistivity as a function of temperature (figure 1.2) showed a logarithmic correction to the Boltzmann conductivity [*Bishop et al* 1980, *Uren et al* 1981]. Here, for a material system previously thought of as quasi-metallic or non activated, there is an increase in resistance at very low temperatures. The scaling theory of conduction [*Abrahams et al* 1979] suggested that all electronic states in two dimensions were

weakly localised in the presence of small but finite amounts of disorder. The weak localisation theory is valid if the distance that an electron travels before being scattered is greater than its Fermi wavelength, i.e. $k_F \ell > 1$, where ℓ is the elastic mean free path and k_F the Fermi wave vector. The correction value at T=0K depends on the length of the sample.

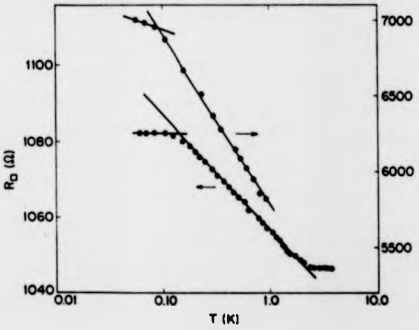


Figure 1.2 Resistance of silicon inversion layers, vs absolute temperature.

After *Bishop et al 1980*

Subsequently, logarithmic corrections either due to localisation or interaction phenomena have been seen in thin metal films [*Bergmann* 1984]. Separation of the correction terms is obtained from magnetoresistance measurements. The interaction contribution to the magnetoresistance is associated with the Zeeman effect which depends on the magnitude of the field, not the direction. The localisation is dependent on the transverse component of the magnetic field. For a 2D system this gives considerable anisotropy in the magnetoresistance (figure 1.3). [*Davies et al* 1983]. Observation of a 3D to 2D transition in the temperature dependence of the resistivity

has been shown in a GaAs MESFET(metal-semiconductor field effect transistor) [*Newson et al* 1986]. A similar transition is not possible using a Si:MOSFET due to its inherent mode of operation. Silicon MBE offers the possibility of observing similar weak localisation and interaction phenomena effects in thin doping spikes, and the possibility of tailoring a 3D to 2D transition. Logarithmic corrections to the conductivity of a boron delta layer in silicon have already been investigated [*Mattey et al* 1992b].

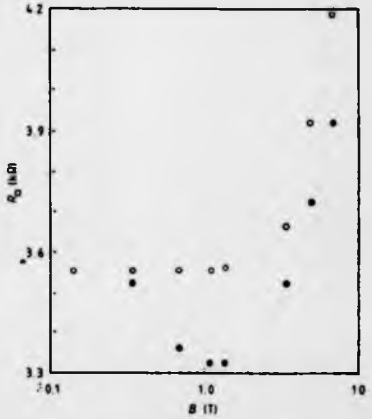


Figure 1.3 Anisotropy of the magnetoresistance for a MOS device. Sample orientation ● Perpendicular and ○ Parallel to the magnetic field. *After Davies et al 1983*

1.4.3 DOPING SUPERLATTICES

The promise of improved device performance through the use of a high mobility structure as the active channel of a device, was first investigated through the use of a MODFET. This is a development of the modulation doped superlattice in which free carriers are spatially separated from their parent atoms. The concept of the superlattice originally proposed by Esaki(1970), who envisaged a periodic potential of period less than the electron mean free path, superimposed on the bulk lattice potential. Here the Brillouin zone is divided into a series of minizones, giving rise to narrow subbands. The superlattice structure could be imposed by a periodic modulation of alloy composition, termed a heterostructure superlattice, or by a periodic variation of donor or acceptor impurities called a doping superlattice. A technical advantage of a doping superlattice(DSL) or a n-i-p-i crystal is that, in principle, any semiconductor can be used as the host material, and restrictions on lattice matching do not apply. There are two approaches to producing a silicon superlattice, (i) Si/SiGe heterostructures, or (ii) a n-i-p-i structure. Doping superlattices appear to offer several unique properties related to a tuneable bandgap and free carrier density via electrical or optical excitation.

The majority of work on DSLs has been in the GaAs system, and is extensively reviewed by Dohler(1987). The band diagram of a n-i-p-i doping superlattice in GaAs is shown in figure 1.4a. The superlattice potential is produced by the space charge modulation of the dopant planes. The band gap, subband structure and carrier concentration are not only affected by the original design parameters, but by voltage tuning through the use of selective contacts to the different type doped layers. Similar effects in silicon doping superlattices have been little studied. This is due in part, to the technological advance of GaAs MBE technology. Previous work on producing a DSL in silicon have produced structures of approximately 75nm period [*Ahlers et al* 1987, *Landheer et al* 1988]. Excess carrier lifetimes have been observed by Landheer *et al*(1988), by making selective contacts to the n and p type layers.

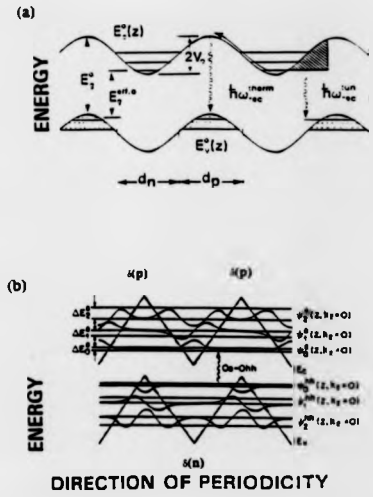


Figure 1.4 (a) Band diagram of n-i-p-i doping superlattice. After *Dohler(1987)*. (b) Sawtooth superlattice. After *Schubert(1989)*

Selective contacting to observe the novel electronic properties has been problematic and has required the use of a shadow masking technique during growth to form ohmic contacts to the layers of interest, i.e. a n-i-n-i doping structure at one end of the DSL and a p-i-p-i structure at the other [*Landheer et al* 1988]. Ion implantation methods, usually favoured for device fabrication, may cause problems due to the number of highly doped tunnelling junctions formed. Hall measurements on Si-DSLs are very

limited. The most noteable results were published by Nakagawa *et al* (1986), who observed a mobility of 40,000 $cm^2V^{-1}s^{-1}$ at 30K, in a type p-i-p-i DSL structure (figure 1.5). This was much higher than equivalently doped bulk material, and thus the p-i-p-i structure appeared to offer enhanced carrier mobilities. {The high mobility DSL had a period of 60nm, and was composed equal widths of p and n-type layers with concentrations of $1x10^{18}cm^{-3}$ and $1x10^{16}cm^{-3}$ respectively. Nakagawa termed the high mobility structure as "p-i-p-i" as the doping in the p-type regions was very much greater than that in the n-type regions.}. Also measured were n-i-n-i and p-n-p-n types of DSL in which no mobility enhancement was found. Theoretical studies of Si-DSL's by Moriarty *et al* (1983) concluded that a higher mobility of carriers could be obtained in a DSL, driven by a reduced conductivity effective mass in a superlattice structure. Further band structure calculations were made by Liwei *et al* (1988).

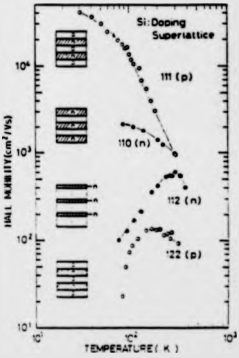


Figure 1.5 Hall mobility of holes and electrons in Si DSL's as a function of temperature. After *Nakagawa et al 1986*

The original Esaki(1970) proposal for a doping superlattice, required that the superlattice potential was of the order of the de-Broglie wavelength in the bulk and that the superlattice period needs to be small in order to couple the electron waves in adjacent wells. The prediction of quantum confined optical transitions was not observed in the DSLs of Dohler(1987). This was due to the inability to produce a strong modulation of the bandgap on a short length scale using homogeneously alternate doped layers. The development of delta doping has since allowed the dopant solid solubility limit to be exceeded. Thus an "Esaki" doping superlattice can be constructed of alternate rows of delta layers of opposite types (figure 1.4b). The resultant profile is then sawtooth shaped. Optical absorption and photoluminescence spectra of GaAs δ-doped superlattices showed clear quantum confined transitions [*Schubert* 1989]. Similar effects have been observed in multiple δ-doped boron layers in silicon [*Park et al* 1991].

1.5 DELTA DOPED TRANSISTOR

The continuing trend of CMOS VLSI circuits has led to minimum device lengths below 0.5μm [*Mulhoff et al* 1991]. Miniaturisation of the device size is limited by two mechanisms: (i) those related to the change in device operation due to the small feature lengths; (ii) those concerning the fabrication of submicron devices. The latter may in general be solved through the use of different lithography techniques, e.g. X-ray, electron beam. However, for submicron gate lengths, short channel effects such as punchthrough, impact ionisation, hot electron effects and impurity fluctuations are fundamental limitations [*Hoeneisen et al* 1972]. A typical example of punchthrough is given by the MOSFET. Reducing the gate length(L) to minimise device area, allows the drain and source depletion regions to be of comparable length to L. If a voltage is applied across the source drain contacts, then as the drain voltage is increased, the drain

depletion region spreads towards the source. Increasing the voltage further, allows the edge of the drain depletion layer to come close to the source depletion region. Thus the potential barrier near to the source is lowered, allowing carriers to be injected in to the depletion layer of the drain, giving rise to an increase in the subthreshold leakage current{ an effect termed Drain Induced Barrier Lowering, see figure 1.6 }.

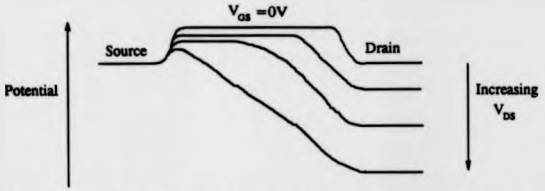


Figure 1.6 Drain induced barrier lowering. Source potential decrease for increasing V_{DS}.

Reducing the depletion widths is possible by decreasing supply voltage and by tailoring the source drain implant profiles. Non-linear doping beneath the gate in a device can be achieved through multiple implants. Channel doping near the surface increases the threshold voltage, while a deep implant can act as a punchthrough stopper. Channel doping is at the expense of reduced carrier mobility due to increased ionised impurity scattering. This scaling of devices to keep electric fields constant places considerable demands on oxide thickness uniformity and reliability. Thus it is possible for devices to exhibit a variation in threshold voltage across a wafer. Impurity fluctuations for 0.1μm gates produce significant threshold voltage shifts across a wafer [*Yamaguchi et al* 1983]. Although scaling devices can in principle keep electric fields constant, the ultimate speed of a short gate device is determined by the saturation drift velocity and the parasitic capacitances.

The use of a delta layer as the conducting channel for a FET was first proposed by Board *et al* (1981), where the conducting carriers are assumed to be confined to the

triangular potential well formed by a delta doping spike. The delta doped field effect transistor (δ-MOSFET) offers significant advantages for submicron applications. Removal of the charge carriers from the oxide interface, reduces hot electron injection into the oxide and may allow a higher mobility due to reduced scattering from interface phonons and interface roughness. The first δ-FET was not realised until Schubert (1985a) produced a δ-doped metal-semiconductor field effect transistor (δ-MESFET) structure in GaAs. The δ-MESFET produced in GaAs showed in principle that there were advantages over a homogeneously doped MESFET, namely high transconductance, a high density of carriers in the 2D gas, large breakdown voltage, reduced short channel effects and easy control of threshold voltage. These advantages also challenge the apparent superiority of the high electron mobility transistor.

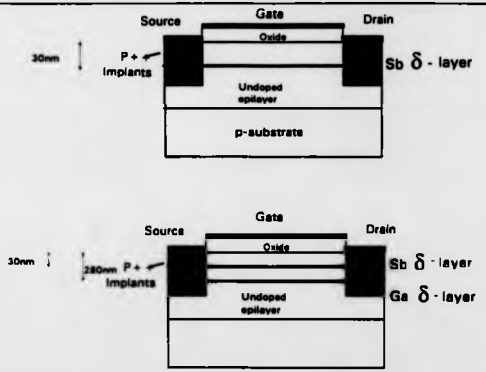


Figure 1.7 (a) Schematic of δ-FET produced by Nakagawa *et al* 1989, (b) Schematic of ALD δ-FET produced by Yamaguchi et al (1988a).

The development of the of GaAs δ-FET has now advanced to the optimisation of device design by using self aligned gates, giving a transconductance of the same order as a

selectively doped heterostructure [*Schubert et al* 1986c]. The development of δ-FET in silicon has been accomplished by Gorkum *et al* (1987), Nakagawa *et al* (1989) using an Sb delta layer as the conducting channel (figure. 1.7a), and by the author, using a boron delta layer, see chapter 5 [*Biswas et al* 1992a]. A silicon δ-MESFET using an Sb channel has also been demonstrated by Zeindel *et al* (1989). However, the device only operated at 4K, and proved impossible to turn off due to a very high delta layer concentration. Later research has concentrated on using a second delta layer, to act as a punchthrough stopper and reduce short channel effects. Yamaguchi *et al* (1983) originally proposed the use of delta layers in a conventional MOSFET to suppress the current flux and confine the potential contours of the drain contact. Modelling of the device showed that punchthrough was completely suppressed for gate lengths down to 0.2μm. This concept was then extended to the δ-FET by Yamaguchi *et al* (1988a), with the devices named by him as Atomic Layer Devices (ALD-MOSFET). These devices consisted of an n-type(Sb) delta layer to act as the conducting channel of the device and a deeper p-type(Ga) channel (figure 1.7b). The second delta layer, deepens the triangular potential well for electrons and suppresses punchthrough. Nakagawa *et al* (1989) has demonstrated that the ALD-MOSFET has a higher transconductance than a Si-MOSFET, but lower than a Si δ-MOSFET. Simulation of an ALD-MESFET [*Yamaguchi et al* 1988b] showed that the use of two punchthrough stoppers for a gate length of 1μm would reduce the residual current to a negligible level compared to δ-FET with only one delta layer punchthrough stopper. For a gate length of 1μm the optimised ALD-FET design includes two p-type punchthrough stoppers (figure 1.8). The model also showed that the transconductance was insensitive to large changes in the concentration of the δ layer.

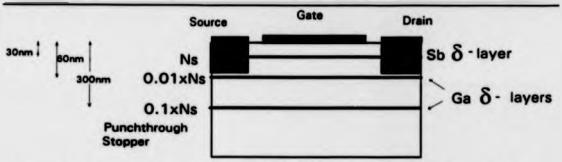


Figure 1.8 Schematic of optimised ALD-MESFET proposed by Yamaguchi *et al* (1988b).

The promise of improved device characteristics has to some extent been demonstrated experimentally, albeit, mainly in the GaAs δ-FET [*Schubert et al* 1986b]. The only systematic theoretical study of δ-FET device parameters in silicon, has been given by Wood & O'Neill(1991). The system studied consists of one delta layer(n or p-type), acting as the conducting channel, with gate lengths of 5μm. The transconductance and threshold voltage variation as a function of delta layer concentration, depth and width is discussed. The charge control analysis of a δ-FET has also been given by Chen *et al* (1991,92). The results were obtained from a self consistent solution of Poisson's and Schrodinger's equation for a triangular shaped well. The use of such techniques though, is questionable, for device operation at 300K, where kT is comparable to the subband separation. The lower mobility in a delta layer in comparison to MOSFET channel would appear not to disadvantage a Si δ-FET with submicron gate dimensions, where the saturation drift velocity determines device speed.

1.6 IN THIS THESIS

This thesis is split into four further chapters, discussing tunnelling spectroscopy measurements on Sb and B delta layers, mobility measurements on doping superlattices and low temperature investigations of quantum corrections to the transport coefficients of narrow doping spikes, and the development of the first p-channel delta doped FET (δ-FET) in silicon. Any study of electrical properties of MBE material relies on the availability of suitable samples. This work has revolved on this limitation.

A doping superlattice study was performed by Hall coefficient measurements on a structure comparable to the high mobility design shown by Nakagawa(1986). Structural analysis has been by secondary ion mass spectrometry, with confirmation of electrical activation by electrochemical capacitance voltage profiles [*Biswas et al 1988*]. With no confirmation of Nakagawa's (1986) high mobility result in a boron doping superlattice, a short study of Sb doping superlattices was performed for enhanced mobility effects.

The two dimensional subband structure of Boron and Antimony delta layers was investigated by tunnelling spectroscopy. The latter system having been previously studied by Eisele (1989) and Li *et al* (1990) was used to confirm the validity of the experimental technique. The discontinuities of the current voltage characteristic, were then compared to theoretical calculations in chapter 2, to allow the identification of the subband energies and to indicate the width of the doping spike [*Biswas et al* 1991].

The electrical transport properties of high resolution doping structures was continued by a study of the low temperature corrections to the conductivity for a thin doped layer(10nm). Similar effects to that observed in a MOSFET structure were seen. Magnetoresistance studies for sample orientations parallel and perpendicular to the field confirmed the two dimensional nature of the doped layer. This also allowed separation of the electron-electron interaction and weak localisation correction terms in the conductivity to be obtained. A transition between two and three dimensional conduction

was then demonstrated by magnetoresistance measurements on doping spikes of widths up to 80nm [*Biswas et al* 1992b].

The practical aspects of a Si-MBE device were investigated by the development of the first boron delta doped field effect transistor [*Biswas et al* 1992a]. A range of device parameters was used to confirm theoretical predictions of device performance. Processing of δ-FET has required the use of a low temperature oxidation process to form a suitable high quality gate dielectric.

Chapter 2 is devoted to the various theoretical concepts used in this work. Models of subband structure in a quantum well are discussed for comparison with tunnelling spectra. Mechanisms of mobility enhancement in a DSL are outlined. Formula for weak localisation and electron-electron interaction corrections to the conductivity at low temperature are detailed. Finally, a model is proposed by the author, which describes the operation of both the long and short gate delta doped FETs.

Chapter 3 concerns all aspects of the experimental work. This includes Hall effect measurements, the cryogenic systems used and experimental techniques developed during this work. Particular attention is paid to sample preparation, in house, or by the use of microfabricated devices from the Edinburgh Microfabrication Facility. In-house sample fabrication was required for Hall measurements, tunnelling spectroscopy and electrochemical capacitance voltage profiling. The logical progression of microfabricated samples with their well defined geometries and known contact regions is shown. This work culminates with the first fabrication of a boron delta FET.

In **Chapter 4**, the results of the experimental work on tunnelling spectroscopy, doping superlattices, weak localisation, electron-electron interactions and magnetoresistance are presented, and discussed using the relevant theories presented in chapter 2. **Chapter 5**: presents results on the boron delta doped FET.

In **Chapter 6**, a summary of the important results is presented, and conclusions drawn, along with suggestions for further work.

CHAPTER 2

THEORY

2.1 TWO-DIMENSIONAL SUBBAND STRUCTURE

The technology of producing nanometre control over dopant profiles with MBE, has allowed a wide variety of quantum confinement effects to be studied. For the simplest dopant profile of a Dirac delta function the charge carriers are confined to an approximately triangular potential well. The space charge potential produced is similar to that of a MOSFET, where by application of suitable electric field, the charge carriers are confined to a narrow inversion layer, which forms an asymmetric triangular well. In such systems the dimensionality is reduced, and the free carriers are restricted to two dimensions(2D). If the thermal de-Broglie wave length is comparable to the spatial extent of this 2-D well, then carrier motion perpendicular to the layer is quantised, into discrete energies. For a silicon inversion layer Ando *et al* (1982) showed that the subband energies take the form;

$$E = E_n + \frac{\hbar^2}{2}\left(\frac{k_x^2}{m_x^2} + \frac{k_y^2}{m_y^2}\right) \qquad (2.1)$$

where k_x and k_y are the wave vector components for motion parallel to the surface and E_n are the electric quantum levels, and m_y,m_x are the principle effective masses for motion parallel to the surface.

Silicon is an indirect gap semiconductor with the valence band maximum at $k=0$ and the conduction band minima along the [100] direction. The lowest conduction

band minimum is at 85% of the way to the Brillouin zone boundary edge. The six constant energy surfaces of the conduction band are ellipsoids with a mass along the major axis of the ellipsoid of m_l=0.916m_o and a transverse mass of m_t=0.190m_o, where m_o is the mass of an electron in free space. Quantisation removes the six fold degeneracy, and the four valleys with a light mass perpendicular to the surface will have higher energy levels according to equation 2.1. The other two valleys are two fold degenerate (see figure 2.1), and lower in energy. Thus for a potential well, the allowed energy levels form a pair of energy ladders that are given the notation $E_{0,1,2,..}$ for the heavy mass and $E'_{0,1,2,..}$ for the light mass. These separate energy ladders are then interleaved with one another, due to the differences in effective mass.

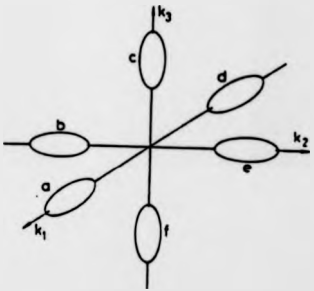


Figure 2.1 Schematic of the constant energy surfaces for the conduction band of silicon.

Carrier motion parallel to the interface is "free" and each subband energy E_n acts as the bottom of a 2-D subband with a constant density of states per unit area and energy.

Therefore the density of states is zero below E_0 and constant for $E > E_0$, up until a second subband is occupied.

The 2-D density of states is given by;

$$D(E) = g_v g_s \frac{1}{4\pi}\left(\frac{2m_d}{\hbar^2}\right) \qquad (2.2)$$

where g_v is the valley degeneracy, g_s the spin degeneracy and $m_d = m_x = m_y$ is the isotropic effective mass per valley.

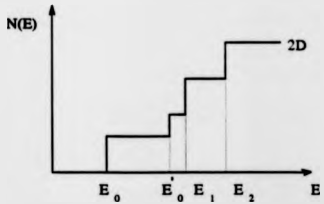


Figure 2.2 The conduction band density of states energy dependence for a 2D energy distribution.

For silicon, the two lower valleys have a density of states effective mass of $0.190m_e$ [*Ando* 1982]. The four fold degenerate valleys have an effective mass in the plane given by $m_d^* = (m_l m_t)^{1/2} = 0.42m_o$. The dependency of the 2D density of states on the effective mass gives a staircase function (figure 2.2). The valence band structure of silicon consists of a maximum located at $k=0$, where two degenerate bands meet, giving rise to light and heavy holes. A third band is also found at $k=0$, but is separated by 0.044eV due to spin orbit splitting. For the present work the valence bands are assumed to have spherical energy surfaces, with approximate effective masses of

$m_h = 0.49m_o$, $m_l = 0.16m_o$ and $m_{so} = 0.24$ where m_{so} is the spin orbit split effective mass. The density of states effective mass for holes is taken as the effective mass of the band.

For a 2D carrier distribution, the total carrier density n_i for the ith subband is given by;

$$n_i = \frac{m^* g_v k_B T}{\pi \hbar^2} \ln\left[1 + \exp\left(\frac{E_F - E_i}{k_B T}\right)\right] \qquad (2.3)$$

and at T=0K, the occupation density is then;

$$n_i = \frac{g_v m^*}{\pi \hbar^2}(E_F - E_i) \qquad (2.4)$$

2.2 CALCULATION OF SUBBAND ENERGIES

The two dimensional subband structure produced by a thin layer of Sb and B dopant atoms has been investigated in this work via tunnelling spectroscopy. Calculations of the subband energies are therefore required to match the observed tunnelling spectra.

Previously, subband energies have been calculated for an asymmetric triangular well as found in heterojunctions or MOSFETs. For example, the lowest subband energy has been calculated by Stern (1972), by a solution of Poisson's and Schrodingers equation. This showed that at T=0K, an inversion layer of concentration $3x10^{12}cm^{-2}$ has only the two lowest subbands E_o ,E_o' occupied.

The impurity distribution of a dopant layer may be considered to be similar to a Dirac delta function (δ) if the layer width is confined to a single atomic plane. Carrier motion is then quantised if this width is comparable to the spatial extent of the thermal de-Broglie wavelength. Classically, the excess free carriers will diffuse from their

parent donors due to diffusion, leaving a corresponding excess of positive charge around the dopant layer.

The conduction band edge profile can be found from Gauss's law, where for a sheet concentration of N_s, located at z=0 (figure 2.3) then [*Schubert et al* 1986b];

$$\frac{dE}{dz} = \left(\frac{q^2}{2\varepsilon}\right) N_s \qquad (2.5)$$

where E is the energy at z. Matching the de-Broglie wavelength (λ_{dB}) to the width of the well gives, for a state of energy E_n;

$$\tfrac{1}{4}(n+1)\lambda_{dB} = \left(\frac{2\varepsilon}{q^2}\right)\left(\frac{1}{N_s}\right) E \qquad (2.6)$$

where n=0,1,2,.....

Solving the above equation gives the subband energies;

$$E_n = \left(\tfrac{1}{4}\right) 2^{-\frac{1}{3}} (n+1)^{\frac{2}{3}} \left[\frac{q^2 2\pi\hbar N_s}{\varepsilon (m^*)^{\frac{1}{2}}}\right]^{\frac{2}{3}} \qquad (2.7)$$

where m^* is the effective mass and $\hbar$ is Planck's constant.

Equation 2.7 neglects the effect of band bending due to free carriers, which will cause the well to not have a strictly triangular shape. Also, the wavefunctions are assumed to have a simple sinusoidal form and do not penetrate the barrier [*Schubert et al 1986b*)

An improvement on the use of a triangular well was proposed by Schubert & Ploog (1985b), and has been used in the present work to calculate the subband energies in an n-type delta layer in silicon. In this improved model the energy of the ground state is calculated from the ground state energy of an infinite potential well, of width $2a_0$ corresponding to $\lambda_{dB}/2$, and matched to the sloping band energy of a triangular well. To calculate the energy of the next subband minimum, a Gaussian surface of width λ_{dB}, enclosing all the free charge in the ground state and the ionised impurity charge is constucted.

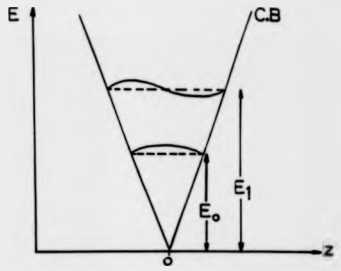


Figure 2.3 Triangular potential well for a delta doped layer

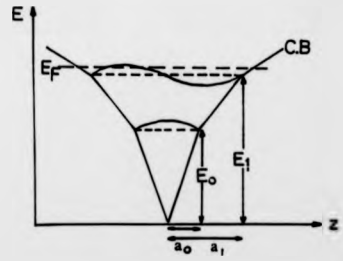


Figure 2.4 Polygonal model of conduction band edge of an n-type delta layer

Thus the field between 0 and a_0 is assumed to be $F = (1/2\varepsilon)qN_s$, where N_s is the areal impurity density. The field between a_0 and a_1 is then:

$$F' = F - \left(\frac{q}{2\varepsilon}\right)n_0 \tag{2.8}$$

where n_0 is the density of electrons(or holes) in the ground state.

$$n_0 = \frac{g_s m^*}{\pi\hbar^2}(E_F - E_0) \tag{2.9}$$

The position of the first subband and the length a_0 can be obtained explicitly from:

$$E_0 = \frac{\pi^2\hbar^2}{8m^* a_0^2} = qFa_0 \tag{2.10}$$

The position of the second subband is modified by screening and is given by:

$$E_1 = \frac{4\pi^2\hbar^2}{8m^* a_1^2} = E_0 + qF'(a_0 - a_1) \tag{2.11}$$

$$E_1 = E_0 + \frac{q^2}{2\varepsilon}(N_s - n_0)(a_0 - a_1) \tag{2.12}$$

Occupation of this subband will in turn screen the higher occupied subbands and lower their energy. In general equation 2.12 is given by:

$$E_i = E_{i-1} + \frac{q^2}{2\varepsilon}\left(N_s - \sum_{j=0}^{i-1} n_j\right)(a_i - a_{i-1}) \tag{2.13}$$

where n_j is the concentration of the electrons in the jth subband. To solve equation 2.13 a cubic equation involving a_i is formed. This is then solved using a Newton-Raphson iterative process.

The calculation proceeds by incrementing the value of E_F untill the neutrality condition given by equation 2.14 is satisfied.

$$N_s = \sum_j n_j \qquad (2.14)$$

The resultant band edge profile is more realistic as screening of the fixed ionised donor (acceptor) charge is included. The well then has a polygonal shape as in figure 2.4. The author has calculated the subband energies for a n-type system in silicon and the results are presented in chapter 4. Schubert *et al* (1986) compared the calculated values for a δ-doped layer in GaAs with experimental Shubnikov-de Haas measurements. The results showed good agreement for the first two subbands. The polygonal model allows quick calculation of the subband energies, However, there are a few limitations that appear more prevalent when higher order energy levels are calculated. For a "deep" well with many subbands occupied, the relative separations of the energy levels appear to "collapse" very quickly. This is partly due to the exclusion of background doping, which if of opposite polarity to the delta layer will change the value of the band bending for states near to the Fermi energy and hence their separation. This effect is most dramatic in the calculated subband energies for a p-type delta layer in silicon, see Mattey *et al* (1992). The suitability of the calculation for tunnelling spectroscopy is limited as the calculation assumes that no tunnelling of the de-Broglie wave out of the quantum well. However, subband calculations can only give broad agreement with most experimental data as various approximations have to be made with the effective masses and boundary conditions used.

The observation of subband structure in a Sb delta layer by tunnelling spectroscopy has led to further calculations of subband structure. Li *et al* (1990) calculated the potential from Poisson's equation and imposed boundary conditions associated with the metal gate and substrate doping level. The assumptions they have used in the modelling are that the delta layer is of finite width but homogeneous in

doping. The electron density for each level is taken as a constant between the corresponding classical turning points. Figure 2.5a shows the results obtained by Li *et al* (1990). Li also investigated whether the gate bias Vg would change the shape of the well, however the resultant change of the subband energies was insignificant compared to their separation. Eisele (1989) also determined the subband energies of a degenerate delta layer by solving self consistently a one dimensional solution of Schrodinger's and Poisson's equation. Figure 2.5b shows Eisele's results for a 1nm homogeneous doping layer, with a background doping of $1x10^{15}cm^{-3}$. Only two subbands appear to occupied for concentrations below $6x10^{13}cm^{-3}$. For dopant widths greater than 2nm, the higher energy levels rapidly become occupied. The agreement of theoretical calculations with experimental data obtained is only very approximate. The author's own attempt at a resonant tunnelling experiment (see chapter 4) also confirmed that there is a problem in identifying the spectra. For almost identical sample parameters of a sheet concentration $N_s = 1.3x10^{13}cm^{-2}$ and a background concentration of $N_A = 5x10^{15}cm^{-3}$ the theoretical results of Li *et al* (1990) and Eisele (1989) are compared to the polygonal model used by the author, see Table 2.1. (Energy levels are given relative to the Fermi energy, blank spaces refer to undetermined energy levels)

TABLE 2.1

COMPARISON OF THEORETICAL CALCULATIONS OF THE SUBBAND ENERGIES OF AN N-TYPE DELTA LAYER RELATIVE TO THE FERMI LEVEL

Ns/ cm^{-2}	Eisele $1.3x10^{13}$	Li $1.3x10^{13}$	Polygonal $1.3x10^{13}$	Eisele $5x10^{13}$	Li $5x10^{13}$	Polygonal $5x10^{13}$
E_0	-55	-35	-55	-110	_	-150
E_0'	-1.9	-7	-15	-45	_	-38
E_1	+37.1	+7	_	_	_	_
E_2	+64.7	+30	_	_	_	_

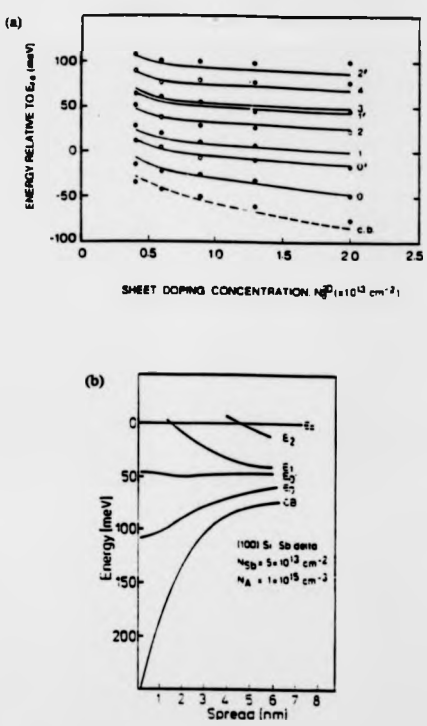


Figure 2.3 (a) Theoretical and Experimental subband energies for an n-type delta layer. After Li et al (1990). (b) Values calculated by Eiselet 1989)

For a quantised n-type layer there is a problem regarding the identity of the first excited state, i.e. is it E_1 or E_0'. This may be demonstrated by calculating the subband energies for an isolated triangular well given by equation 2.7. For a sheet density of $1.3\times10^{13}cm^{-2}$, the subband energies are calculated as $E_0=99meV$, $E_0'=168meV$ and $E_1=158meV$. Thus this calculation gives a different order to the energy levels, in that there are two heavy electron states before the first light electron state. Tunnelling spectroscopy of a 100 surface by Kunze(1984) identified the first excited state as E_0'. Theoretical models of Stern (1982) found the opposite effect, and that E_1 was the first excited state. For the purpose of calculating the energies in the polygonal model, E_0' was taken as the first excited state.

2.3 TUNNELLING SPECTROSCOPY

The 2D subband structure at an inversion layer for the Si-SiO_2 interface has been extensively studied [*Ando* 1982]. Optical characterisation by infrared spectroscopy does not allow the determination of the Fermi level, and only optical k-conserving transitions are allowed. Tunnelling spectroscopy by measurement of the tunnelling current through a thin barrier has been used to determine the subband energies of 100 and 111 Si inversion surfaces [*Kunze* 1984]. According to Bardeen(1961) the tunnelling current is:

$$I \propto \sum_{\mu,\nu} f(E_\mu)\left[1-f(E_\nu+eV)\right]\left|M_{\mu,\nu}\right|^2 \delta(E_\mu - E_\nu) \qquad (2.15)$$

where f(E) is the Fermi function, V the applied bias, δ the Dirac delta function and $M_{\mu,\nu}$ is the tunnelling matrix element between states Ψ_μ in the metal gate and Ψ_ν in the semiconductor. Considering the case of tunnelling through a Schottky barrier in to a

delta layer(figure 1.1). At low temperatures, small voltage biases and assuming the density of states is independent of E, an approximate expression for the current is [*Wolf* 1985]:

$$I \propto \sum_n \int_0^{eV} N(E - E_n)\, T(E, E - E_n)\, dE \qquad (2.16)$$

where $N(E-E_n)$ is the 2D density of states, and T is the transmission coefficent of the electrons in the the nth subband. Differentiating (2.16) gives:

$$G = \frac{dI}{dV} \propto \sum_n N(eV - E_n) \qquad (2.17)$$

This simple expression suggests that the conductance G when plotted against V will have a staircase shape. However, this ignores though the voltage dependence of T and of the shape of the well, which leads in practice to a series of peaks in G, which are superimposed on a rapidly varying background.

2.4 PARALLEL TRANSPORT IN DOPING SUPERLATTICES

The production of a high mobility structure that may be used as a basis of a high speed transistor has been mainly been sought through the use of modulation doped heterostructures. The SiGe system allows the production of a heterostructure in silicon, and enhanced hole mobilities effects have been observed by People *et al* (1984) and enhanced electron mobilities by Abstreiter *et al* (1985). The production of an enhanced mobility structure using a doping structure in a homoepitaxial system is comparatively little investigated. Shannon(1980) predicted that carrier spillage from a thin highly doped region into a thick low doped region may increase the speed of a device. Here the carriers "spilled" in to the low doped regions experience fewer ionised impurity collisions centres thus increasing the mobility of these carriers. Thus, it is expected that enhanced mobility effects will be found in a high/low doping superlattice structure.

This is unlike the DSL's investigated by Dohler(1987) where a compensated structure of both P and N-type doping produces the periodic potential, see chapter 1.4.3. Here free carriers are in the same region of space as their parent donors. The high/low interface between two different impurity concentrations in a DSL, produces a sharp concentration gradient of charge carriers. These are then free to diffuse from the higher to the lower concentration regions. Diffusion continues until an equilibrium is achieved between the diffusion potential and the resultant electric field. Over the whole superlattice the structure will be electrically neutral, but this will not be the case within a few Debye lengths of the impurity concentration gradient, where the Debye length is given by:

$$L_D = \sqrt{\frac{\varepsilon\varepsilon_0 kT}{q^2 N_L}} \qquad (2.18)$$

where N_L is the concentration of the low doped regions. Then for a high/low structure with a doping concentration of $10^{18}cm^{-3}/10^{15}cm^{-3}$ at 300K, the carriers will diffuse in to the low doped region over a distance > 130nm.

The actual free carrier profile of the DSL may be obtained from a solution of Poisson's equation:

$$\frac{d^2\phi}{dx^2} = \frac{q^2}{\varepsilon\varepsilon_0}\left(N^+(x) - n(x)\right) \qquad (2.19)$$

where $\phi(x)$ is the potential, $N^+(x)$ is the ionised impurity concentration and $n(x)$ the density of the electrons in the conduction band. The contribution of the minority carriers (holes) is assumed to be negligible. Equation 2.19 can be solved via an iterative process as both the potential profile and the carrier density are a function of the distance x.

An n-type doping superlattice consisting of a periodic sequence of 2nm at $10^{19}cm^{-3}$ and 20nm at $10^{15}cm^{-3}$ has been solved by O'Neill(1987). The carrier concentration was found to vary between $2.6x10^{18}cm^{-3}$ and $4.2x10^{17}cm^{-3}$ (see figure 2.6a). This structure appears to give $10^{2}cm^{-3}$ extra carriers located in the low doped

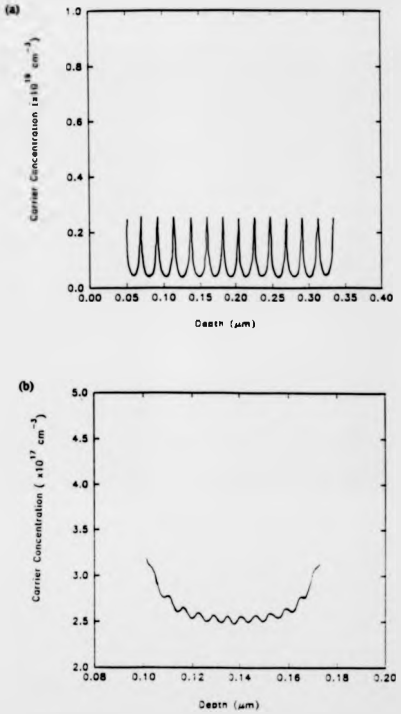


Figure 2.6 (a) Plot of carrier concentration in a high/low DSL consisting of 2nm at $1x10^{19}cm^{-3}$ and 20nm at $1x10^{15}cm^{-3}$. (b) repeated for DSL of 3nm at $5x10^{17}cm^{-3}$ and 3nm at $1x10^{15}cm^{-3}$.

3Pa

regions. The calculation was repeated for a DSL consisting of 3nm at $5x10^{17}cm^{-3}$ and 3nm at $1x10^{15}cm^{-3}$. The carrier concentration in this structure stays at approximately $2.5x10^{17}cm^{-3}$ (figure 2.6b) so some mobility enhancement might be expected, as half of the structure is lightly doped. As discussed earlier in chapter 2.1, the formation of discrete subbands leads to a change in the effective mass used to describe transport properties. For the case where the doubly degenerate band is occupied then the effective mass in the plane of the DSL is $0.190m_o$. Moriarty *et al* (1982) discussed mobility enhancement in a silicon superlattice based on the reduced conductivity effective mass. Thus if the bulk conductivity effective mass is $0.26m_o$ then a 27% decrease in the electron effective mass is found for [100] orientated superlattices. Krishnamurthy extended the calculations to suggest possible mobility enhancement of 1.17 in the impurity scattering limit and 2.20 in the phonon scattering limit, for doping concentrations in excess of $10^{18}cm^{-3}$. The superlattices considered a periodic potential produced by alloy composition or by n-i-p-i DSL, however alloy scattering and modulation doping effects were neglected.

Delta doping may also lead to enhanced mobility effects. Carriers in the well have high Fermi energies (and Fermi velocities) are therefore less easily scattered by impurities. Furthermore, carriers in odd numbered subbands ($n=1,3,5$ with the corresponding number of wavefunction modes) have zero probability of being found in the plane of the dopant sheet [*Schubert et al* 1987]. Schubert also proposed that screening of the impurity charges by the high concentration in the delta doped well, may also have some affect on the mobility of carriers.

2.5 THE HALL EFFECT

The force experienced by an electron in the presence of an electric field E and a magnetic field B is given by the Lorentz equation $\underline{F} = -e(\underline{E} + \underline{v} \wedge \underline{B})$. The rate of momentum change per electron is then:

$$\frac{d\underline{p}}{dt} = -e(\underline{E} + \underline{v} \wedge \underline{B}) - \frac{m\underline{v}}{\tau} \qquad (2.20)$$

where v is the average velocity. The components of the velocity (v) in the steady state is found from equation (2.20) as:

$$v_x = \mu(E_x - v_y B)$$
$$v_y = \mu(E_y + v_x B)$$
$$v_z = \mu E_z = 0$$

For the Hall plate shown in figure 2.7, the Lorentz force drifts an electron in a direction orthogonal to both $\underline{E}$ and $\underline{B}$ vectors and the Hall field E_y compensates for the y component of the force. Using Ohm's law $\underline{J} = \sigma\underline{E}$ defines the linear relationship between $\underline{E}$ and the current density $\underline{J}$.

$$J_x = \sigma\frac{\left[E_x - \mu B E_y\right]}{1 + \mu^2 B^2} \qquad \text{and} \qquad J_y = \sigma\frac{\left[E_y + \mu B E_x\right]}{1 + \mu^2 B^2}$$

For no load connected across the Hall terminals, then $J_y = 0$ and the Hall coefficient (R_H) is defined by $E_y = -R_H J_x B$. The Hall coefficient is related to the carrier density (n) by $R_H = r/qn$. Here r is the Hall scattering factor which is equal to $\langle\tau^2\rangle/\langle\tau\rangle^2$, where τ is the mean time between collisions for the carriers. For silicon, r may take values between 0.7 and 1.8 dependent on carrier type and concentration and temperature [*Sasaki et al* 1988]. Typically r is taken as equal to 1, and this is acknowleged by calling the deduced mobility as the Hall mobility, which is given by $\mu = R_H\sigma$.

However for B≠0 the resistivity and conductivity parameters become tensors, such that the resistivity tensor is the reciprocal of the conductivity but elements of the resistivity tensor are not reciprocals of the conductivity. In two dimensions the current density is given by;

$$\begin{bmatrix} J_x \\ J_y \end{bmatrix} = \begin{bmatrix} \sigma_{xx} & -\sigma_{xy} \\ \sigma_{yx} & \sigma_{yy} \end{bmatrix} \begin{bmatrix} E_x \\ E_y \end{bmatrix} \qquad (2.21)$$

The resistivity may then be expressed as:

$$\rho_{xx} = \frac{\sigma_{xx}}{\sigma_{xx}^2 + \sigma_{yx}^2} \qquad \text{and} \qquad \rho_{yx} = \frac{-\sigma_{xy}}{\sigma_{xx}^2 + \sigma_{yx}^2} \qquad (2.22)$$

Thus if $\rho_{xy} = 0$ then $\rho_{xx} = \sigma_{xx}^{-1}$ which is expected for B=0. For a large Hall bar (figure 2.7) where L>>W and where $J_y = 0$,the measurable quantities are ρ_{xx} and ρ_{xy} obtained by;

$$\rho_{xx} = \frac{E_x}{J_x} \qquad \text{and} \qquad \rho_{xy} = -\frac{E_y}{J_x} \qquad (2.23)$$

The magnetoresistance is determined by measuring ρ_{xx} in the presence of a magnetic field. For a low Hall mobility and μB small then, $\sigma_{xx}(B) \approx 1/\rho_{xx}(B)$.

For a two layer system such as would be found in a high-low doping structure, in which regions of low carrier density and high mobility are embedded in regions of low mobility, high carrier concentration material (see section 2.4), the Hall coefficient is given by Schroder (1990) as:

$$R_H = \frac{1}{\left[\left(\sigma_1^2 R_{H1} t_1 + \sigma_2^2 R_{H2} t_2\right) + R_{H1} R_{H2} \sigma_1^2 \sigma_2^2 \left(R_{H1} t_2 + R_{H2} t_1\right) B^2\right]} \qquad (2.24)$$
$$\left(\sigma_1 t_1 + \sigma_2 t_2\right)^2 + \sigma_1^2 \sigma_2^2 \left(R_{H1} t_2 + R_{H2} t_1\right)^2 B^2$$

where $t = t_1 + t_2$ is the thickness of the layers (figure 2.7). For weak magnetic fields, the B^2 terms are small and R_H is given by;

$$R_H = \frac{t\left(R_{H1}\sigma_1^2 t_1 + R_{H2}\sigma_2^2 t_2\right)}{\left(\sigma_1 t_1 + \sigma_2 t_2\right)^2} = \frac{t\left(n_1\mu_1^2 t_1 + n_2\mu_2^2 t_2\right)}{q\left(n_1\mu_1 t_1 + n_2\mu_2 t_2\right)^2} \qquad (2.25)$$

For high fields R_H is given by;

$$R_H = \frac{tR_{H1}R_{H2}}{R_{H1}t_2 + R_{H2}t_1} \qquad (2.26)$$

Using the above equations it is possible to deconvolute the contributions of the different carriers as a function of magnetic field. The analysis though requires the carriers to be of opposite type [*Lou et al* 1984] or the ratio of the mobilities of the carriers to be very large, as in high electron mobility heterostructure. In the present work, the epilayer samples under investigation have been grown substrates of the opposite carrier type to eliminate parrallel conduction paths. However, the above discussion will prove useful in the discussion of high/low doping superlattice structures.

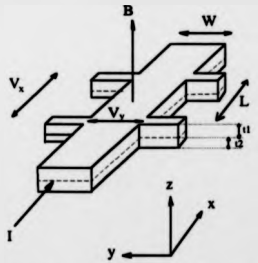


Figure 2.7 Hall Bar sample geometry.

2.6. CORRECTIONS TO THE BOLTZMANN CONDUCTIVITY

2.6.1 LOCALISATION AND QUANTUM INTERFERENCE PHENOMENA

For solids in which carrier scattering due to disorder is weak, corresponding to $k_F\ell$ very much greater than 1, the electrical conductivity σ is given to a good approximation by $\sigma = ne\mu$ where n is the carrier concentration per unit volume, e is the electronic charge and μ is the mobility. If τ is the time between elastic scattering process then $\mu = e\tau/m^*$ where m^* is the effective mass. The elastic scattering time is related to the mean free path ℓ by $\ell = v_F\tau$ where v_F is the Fermi velocity, but requires that the de-Broglie wavelength of the carrier is less than ℓ.

The electronic charge transport property of reduced dimensionality structures has mainly been studied in the MOS and heterojunction systems. In the former, carriers are confined to a thin space charge layer due to the inversion of the surface by a gate electrode. An extensive review is given by Ando *et al* (1982). Dohler (1978) proposed that a thin homogeneous doping spike, buried within the bulk semiconductor crystal would show similar reduced dimensionality effects.

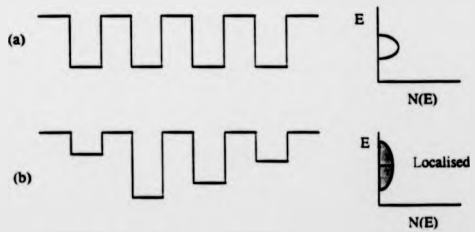


Figure 2.8 (a) Ordered lattice with equal potential wells. (b) Disordered well with distribution V_o

Carrier scattering in an inversion layer can be strong due to the presence of appreciable disorder at the Si/SiO_2 interface, oxide charges and interface states. Anderson (1958) showed that for sufficiently strong disorder the electron wavefunction becomes localised and decays exponentially with distance. He considered a tight binding band of width B formed from a random series of equally spaced potential wells of depth distribution V_o (figure 2.8). If the dimensionless disorder parameter V_o/B was greater than some critical value then the solution to Schrodingers wave equation was no longer extended Bloch waves, but decayed exponentially with distance r as $\exp(-\alpha r)$. Thus for small values of B localisation will occur, corresponding to weak coupling between the wells. Mott {reviewed in Mott 1974} extended the argument for the case where disorder was not sufficiently strong to localise all the states in the band. Here an energy exists termed the mobility edge E_C which separates extended states from localised states in the band tail (figure 2.9).

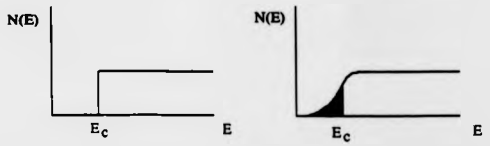


Figure 2.9 (a) 2D Density of states for an unperturbed system. (b) Disorder introducing localised states in band tail.

If at absolute zero the Fermi level E_F drops below E_C , then the conductivity drops to zero discontinuously from a finite value termed the minimum metallic conductivity σ_{min}, which is given by;

$$\sigma_{min} = \frac{0.05e^2}{\hbar a} \quad \ldots\ldots 3D$$

$$\sigma_{min} = \frac{0.1e^2}{\hbar} \quad \ldots\ldots 2D$$

Using an MOS device it is possible to move E_F through E_C to observe the transition between localised states and extended states. If E_F passes through E_C a metal-insulator transition is said to occur. At low temperatures where $E_F < E_C$ conduction occurs via hopping between localised states and then by variable range hopping as the temperature is decreased further. This process is a combination of tunnelling and thermal activation. The conductivity is then determined by hopping probability given by $\exp(-2\alpha R + W/kT)$, where R is the hopping distance. $1/\alpha$ is the decay constant of the wavefunction and W is the hopping energy required. For variable range hopping in 2D $\sigma \propto T^{-1/3}$. Increasing the temperature, increases the carrier concentration above E_C and conduction is then by excitation to these extended states. All these conduction processes have been observed in silicon inversion layers{see Ando 1982}. A weak temperature dependence of the conductivity is also found for E_F above E_C. This observation demonstrates that weak localisation occurs for all states in 2D and was predicted by Abrahams, Anderson, Licciardello and Ramakrishnan (1979) who extended the scaling theory of localisation proposed by Thouless (1977). The scaling theory predicts that there is no discontinuous metal-insulator transition, rather that there is a continuous one in three dimensions and that all states are localised in two dimensions. The T=0K conductivity was found to be dependent on the sample size and not on an intrinsic property of the sample. The results are summarised by Lee & Ramakrishnan(1985). For a 2D system the length dependent conductivity is given by:

$$\sigma(L) = \sigma_0 - \frac{e^2}{\pi^2 \hbar} \ln\left(\frac{L}{l}\right) \qquad (2.27)$$

where σ_B is the Boltzmann conductivity, L is the sample length and ℓ is the mean free path for elastic scattering. Thus at T = 0, L = sample size so $\sigma \to 0$ as $L \to \infty$ and all states are localised. At finite temperatures the corresponding correction to the conductivity has been calculated for $k_F \ell >> 1$. A physical picture of the process relates to the quantum interference of an electron wave proposed by At'lshuler and Aronov (1985). Figure 2.10 represents an electron diffusing between two points A and B in an extended system, making elastic collisions with impurities.

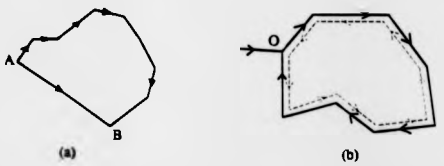


Figure 2.10 (a) Representation of an electron diffusing between two points A and B taking two different paths (b) Closed path for an electron diffusing via elastic collisions to one coincident point O.

The electron may take several different paths between the two points. For two points that coincide (figure 2.10) and with two paths that are of the same length , the wave function will constructively interfere. The probability of finding an electron at any point is then the square of the sum of the wavefunction amplitudes for each path. Thus, interfering waves must be phase coherent for this effect to occur.

$$P = \left| \sum_i \Psi_i \right|^2 = \sum_i |\Psi_i|^2 + \sum_{i \neq j} \Psi_i \Psi_j^* \qquad (2.28)$$

The right hand term of 2.28 represents the quantum interference correction. Typically the latter term involves different paths and phases so the terms sum to zero. For clockwise and anticlockwise diffusion round a closed loop, the two electron waves will be in equal in amplitude and phase coherent back at the origin. Thus the probability of finding an electron at O is given by;

$$\Psi_1^2 + \Psi_2^2 + \Psi_1\Psi_2^* + \Psi_2\Psi_1^* = 4|\Psi_1|^2 \qquad (2.29)$$

The result shows that the probability of finding an electron at O, is twice the value of two phase incoherent waves. This then corresponds to a reduction in the diffusion constant and a reduction in the conductivity, as compared to the Boltzmann theory which treats the diffusion as classical. { The diffusion coefficient D of the electron is related to the conductivity by the Einstein relation $\sigma = e^2DN(E_F)$ where $N(E_F)$ is the density of states at the Fermi level }. So far only the T=0 dependence has been discussed, where the relevant length scale is the sample length L. At finite temperatures, inelastic scattering processes result in the destruction of the phase coherence of the electron wave, with a phase relaxation time of τ_ϕ, in a distance less than L. The phase breaking length is defined as $L_\phi = \sqrt{D\tau_\phi}$ and is the distance over which the phase coherence is maintained, where D is the diffusion coefficient. Thouless(1977) proposed that any inelastic process destroys the phase coherence. Thus the length scale is the inelastic scattering length L_i defined as: $L_i = \sqrt{D\tau_i}$. If $\ell = \sqrt{D\tau}$, where τ is the elastic scattering time, then from equation 2.28:

$$\sigma = \sigma_B - \frac{e^2}{2\pi^2\hbar}\ln\left(\frac{\tau_i}{\tau}\right) \qquad (2.30)$$

If τ_i depends on the temperature T, as $\tau_i \propto T^{-p}$, and τ is independent of T then the conductivity varies as lnT.

$$\sigma = \sigma_B + \frac{pe^2}{2\pi^2\hbar}\ln\left(\frac{T}{T_o}\right) \qquad (2.31)$$

where p is the temperature exponent of the scattering mechanism.

The logarithmic temperature dependence of the conductivity has been observed in thin metal films [*Bergmann* 1984] and Si inversion layers [*Bishop et al* 1980, *Uren et al* 1981].

The dimensionality of the system is determined by the magnitude of L_ϕ .Thus if t is the thickness of the system then: for $L_\phi > t$, 2D behaviour is found and for $L_\phi < t$ the system is 3D. For a 3D system the conductivity is given by (Lee & Ramakrishnan 1985) as;

$$\sigma_{3D} = \sigma_0 + \frac{e^2}{\hbar \pi^2 a} T^{p/2} \qquad (2.32)$$

2.6.2 ELECTRON-ELECTRON INTERACTIONS

The electron-electron interactions in a disordered metal is enhanced by virtue of (a) scattering by impurities which correlates the motion of the electrons, (b) by quantum interference which leads to enhanced probability to find two electrons at a point (Al'tshuler and Aronov 1985). The interaction consists of a Hartree term involving electrons of antiparallel spin and an exchange term involving electrons of parallel spins and leads to a minimum in the density of states at the Fermi level.

Bergmann(1988) has discussed two electrons transversing a loop in the same direction(e.g. clockwise) by a series of scattering events to interfere constructively at the origin. The electrons are dephased in a time $\hbar/kT$ due to the Fermi surface which reduces the strength of the interaction and leads to a temperature dependent conductivity;

The logarithmic correction to the temperature dependent conductivity is given by Lee & Ramakrishnan (1985) for $k_F l > 1$ as;

$$\delta\sigma_t = \left(2 - \tfrac{1}{2}F^*\right)\frac{e^2}{4\pi^2\hbar}\ln\left(\frac{T}{T_e}\right)\cdots\cdots 2D \qquad (2.33)$$

$$\delta\sigma_t = \frac{1.3}{\sqrt{2}}\left(\tfrac{1}{2} - \tfrac{1}{2}F^*\right)\frac{e^2}{4\pi^2\hbar}\sqrt{T/D}\cdots\cdots 3D \qquad (2.34)$$

where F^* is screening parameter.

The associated thermal coherence length is $L_T = \sqrt{\hbar D/kT}$, and a film is two dimensional for interactions if the thickness of the film is $< L_T$.

For small weak localisation and interaction terms the correction to the conductivity is additive, and in 2D this gives:

$$\sigma(T) = \sigma(T_e) + \frac{e^2}{2\pi^2\hbar}\left[\alpha p + \left(1 - \tfrac{3}{4}F^*\right)\right]\ln\left(\frac{T}{T_e}\right) \qquad (2.35)$$

Thus the logarithmic dependence of the conductivity leads to difficulty in separating the weak localisation and Interaction terms. With two characteristic lengths for the sample at low temperatures it is possible for a film to be 2D for localisation and 3D for interactions.

2.6.3 MAGNETIC FIELD DEPENDENCE OF QUANTUM CORRECTIONS

If a transverse magnetic field is applied to a 2D system, then the phase coherence of the clockwise/anticlockwise waves transversing the scattering loop is affected. The phase change is given by:

$$\Delta\phi = \frac{2eB.A}{\hbar} \qquad (2.36)$$

where A is the vector surface area of the scattering loop. Thus an increasing magnetic field destroys the constructive interference giving the weak localisation and the

conductivity increases. The magnetoconductivity for a transverse magnetic field is given by Hikami *et al* (1980) as:

$$\Delta\sigma_L(B) = \frac{n_v \alpha e^2}{2\pi^2 \hbar}\left[\psi\left(\frac{1}{2}+\frac{1}{a\tau_s}\right) - \psi\left(\frac{1}{2}+\frac{1}{a\tau}\right) + \ln\left(\frac{\tau_s}{\tau}\right)\right] \qquad (2.37)$$

where $a = 4eB/\hbar$, ψ is the digamma function, and n_v is the valley degeneracy, eg. 2 for an n-type silicon layer. For a parallel field, the loop area in the field is zero, so no negative magnetoresistance is predicted. This then allows confirmation of the two dimensionality of a sample to be verified by the anisotropy in the magnetoresistance.

The effect of a magnetoresistance on the interactions is dependent on the orientation of the spinning electrons. Using Bergmann's model of the two electrons transversing a closed loop, no change in phase is induced for the two electron waves. However a difference in energy is induced between the spin up and down electrons. This Zeeman spin splitting, if greater than kT dephases the electron pairs giving a negative contribution to the Hartree term with a consequential increase in resistance. The exchange term is independent of the field strength as the electron pairs considered have the same spin orientation. Since the correction is dependent on the magnitude of the field and not orientation, it is possible to separate it from the weak localisation term, by measurement of the correction in a sample in the plane of a magnetic field. The 2D Zeeman correction term for interactions is given by Lee and Ramakrishnan (1985) as;

$$\Delta\sigma_t(B) = -\frac{e^2 F^*}{4\pi^2 \hbar} G(h) \qquad (2.38)$$

where $h = g_L \mu_B B/kT$, g_L is the Landé g factor and μ_B is the Bohr magneton.

Another indication of the interaction mechanism is in the Hall coefficient. Al'tshuler, Aronov and Lee (1980) showed that there was no correction in the σ_{xy}, which leads to a correction in R_H, with δR_H varying as

$$\frac{\delta R_H}{R_H} = \frac{-2\sigma_{xx}}{\sigma_{xx}} = \frac{-2\delta R}{R} \qquad (2.39)$$

The correction δR_H is zero in the single electron quantum interference case, so that measurement of the Hall coefficient and the temperature dependence of the conductivity may be used to determine α_P and F^σ as has been demonstrated by Uren *et al* (1981).

2.7 THE DELTA DOPED FET

Theoretical modelling of the characteristics from a silicon δ-FET has been accomplished by Chen (1991) and Wood *et al* (1991). These have been obtained using various computer modelling packages. Although useful data are obtained on the general trend of characteristics due to the variation of delta doping parameters, no quantitative expressions for the device are presented. The exact operation of the device is still unclear, i.e. does the δ-FET operate as a MOS device where the charge in the delta channel is modified or does the device behave similar to a MESFET, where the depletion width of the conducting channel is modulated. To extract useful information from the boron δ-FET a model has been developed by the present author, which is presented here. Device parameters such as the mobility and transconductance may easily be extracted from the experimental data obtained in this work. It will be shown that the derived expressions are very similar to that of a Si-MOSFET.

2.7.1 GENERAL ANALYSIS

Figure 2.11 shows a schematic model of a delta doped FET. Here the delta layer is assumed to have a finite width of a, but which is nevertheless much less than its depth below the SiO_2/Si interface, so that the gate electrode can be treated as one plate of a parallel plate capacitor. Typical device parameters have the oxide thickness t_{ox} approximately equal to the cap thickness t_s , where $Ts >> tox, ts$, and where Ts is the distance between delta layer and the back of the substrate. Charge modulation then occurs in the upper depletion region of the delta layer, as the capacitance of the Si cap+oxide is assumed greater than the capacitance of the delta layer to the back of the substrate.

The gradual channel approximation is used, where the length of the channel is $L >> a$, which allows V(x) to be linear along the channel length and where $0 \le V(x) \le V_D$. The areal density of charge in the upper depletion region (figure 2.12), assuming $\omega_2 << \omega_1$ and $\omega \approx \omega_1$, is given by;

$$\sigma(x) = \omega(x) q N_D$$

$$\sigma(x) = C(V(x) - V_G) \qquad (2.40)$$

where $\omega(x)$ is the width of the depletion region. V_G is the gate bias, σ is the areal density of charge, N_D is the 3D concentration of dopant in the channel, assumed constant.

The capacitance C is given by:

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_s}\right)^{-1} = \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_s}{\varepsilon_s}\right)^{-1} \qquad (2.41)$$

where t_{ox} = gate oxide thickness
t_s = silicon cap thickness
C_{ox}, C_s = capacitance's per unit area of oxide and silicon
$\varepsilon_{ox}, \varepsilon_s$ = relative permittivities of oxide and silicon

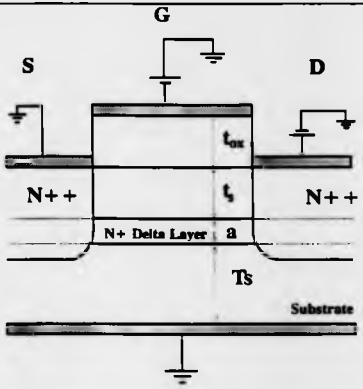


Figure 2.11 Schematic model of delta-FET

and the width of the conducting channel is then $\cong a - \omega(x)$

$$dV = IdR = \frac{Idx}{qN_D\mu W(a-\omega)} \tag{2.42}$$

where W = gate width

μ = mobility

Integrating equation 2.42 to obtain I_{DS}:

$$\int_0^{V_{DS}} (a-\omega)dV = \int_0^L \frac{Idx}{qN_D\mu W} \tag{2.43}$$

Substituting 2.40 and integrating gives:

$$I_D = \frac{qN_D\mu W}{L}\left[aV_D - \frac{C}{qN_D}\left(\frac{V_D^2}{2} - V_G V_D\right)\right] \qquad (2.44)$$

The analysis used is now similar to that for Junction Field Effect transistor: Calculate $I_D = I_{DS}$ at pinchoff, $V_D = V_{DS}$. Assume that it remains constant for $V_D > V_{DS}$.
The pinchoff voltage V_p is then obtained from 2.41

$$V_p = \frac{aqN_D}{C} \qquad (2.45)$$

Then substituting into (2.44)

$$I_{DS} = G_o\left((V_G + V_p) - \frac{1}{V_p}\left\{\frac{1}{2}(V_G + V_p)^2 - V_G(V_G + V_p)\right\}\right) \qquad (2.46)$$

where $G_o = N_D\frac{q\mu Wa}{L}$

The transconductance is given by; $g_m = \left(\frac{\partial I_{DS}}{\partial V_G}\right)_{V_{DS}} = G_o\left(1 + \frac{V_G}{V_p}\right)$ (2.47)

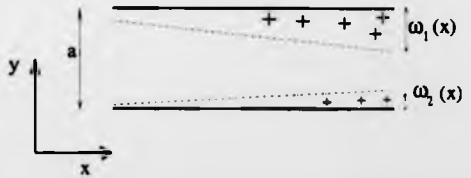


Figure 4.12 Schematic model of delta-FET channel, where a is the width of the delta channel, and ω(x) are the widths of the depletion regions.

Equation 2.46 can be rewritten as:

$$I_{DS} = \frac{\mu WC}{2L}(V_G + V_P)^2 \qquad (2.48)$$

This can now be compared with the saturation current I_{DS} of a MOSFET ;

$$I_{DS} = \frac{\mu WC}{2L}(V_G - V_T)^2 \qquad (2.49)$$

where V_T is the threshold voltage. Equations 2.47 & 2.48 are used to analyse the experimental results of the present author, shown in chapter 5.

For small channel lengths(short gate), where the saturation velocity of electrons dominates, the saturation current is given by:

$$I_{DS} = N_D v_s q W(a - \omega) \qquad (2.50)$$

From 2.47 and 2.45 the transconductance is:

$$g_m = v_s W\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_s}{\varepsilon_s}\right)^{-1} \cong \frac{\varepsilon_{ox} v_s W}{t_{ox}} \qquad (2.51)$$

Using a MESFET model, i.e. assuming no oxide capacitance the transconductance is then:

$$g_m = \frac{\varepsilon_s v_s W}{t_s} \qquad (2.52)$$

where t is the silicon cap thickness. This expression is then identical to that derived by Board *et al* (1981) for a saturation velocity limited model.

The parameters for an optimised δ-FET can be found from (2.47) and (2.52):

1. small t_s or gate length
2. High mobility or saturation velocity
3. High delta concentration.

CHAPTER 3

EXPERIMENTAL TECHNIQUES

3.1 GROWTH BY SILICON-MOLECULAR BEAM EPITAXY

The layers studied in this work were produced on two commercial molecular beam epitaxy machines (V80 & V90S). A description of the silicon MBE growth process has been well documented in the reviews of Kasper (1988) and Kubiak *et al* (1988). The layers in this work were grown to the author's specifications.

Si-MBE technology has advanced during the course of this work, with the result that nanometre control of dopants can now be realised using delta doping. This has been achieved through technological advances as well as a greater understanding of doping kinetics [*Kubiak and Parry 1991*]. A comparison of the advance in Si-MBE can be made by studying the First International Symposium on Si-MBE(1985) and the recent MRS symposium 1991 on Si-MBE.

The first structures studied in this work used the results of boron doping experiments by Kubiak *et al* (1985), which allowed the growth of superlattices with periods of 60nm. It is now possible through the use of delta doping to achieve superlattice periods of 4nm or less.

3.1.1 GROWTH OF BORON DOPING SUPERLATTICES

To confirm the Hall mobility results obtained by Nakagawa(1986) and to seek an explanation of the behaviour, (introduced in chapter 1.4.3), a range of boron doping

superlattices were grown using the basic design of Nakagawa's high mobility structure. The doping superlattices consisted of ten boron doping spikes of width 30nm separated by $1x10^{16}cm^{-3}$ Sb doped layers of 30nm. The wafers were grown using the coevaporation doping technique developed by Kubiak *et al* (1985). A growth rate of $0.3nm\ s^{-1}$ and a substrate temperature of 760°C was used. The wafer specifications are given in table 3.1, and a growth schematic in figure 3.1.

TABLE 3.1

GROWTH SPECIFICATIONS OF BORON DSL's

Wafer ID	N_A /cm^{-3}	N_D /cm^{-3}	d_n /nm	d_p /nm	No. of Periods	Substrate type
68.7	$1x10^{18}$	$1x10^{16}$	30	30	10	n-
68.9	$1x10^{18}$	$1x10^{16}$	30	15	10	n-
68.10	$1x10^{18}$	$1x10^{16}$	30	60	10	p-

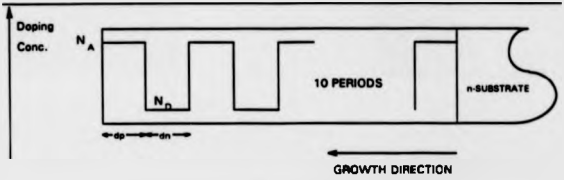


Figure 3.1 Schematic of boron doping superlattice.

3.1.2 GROWTH OF ANTIMONY DOPING SUPERLATTICES

The antimony doping superlattices were grown using the technique of potential enhanced doping (PED) [*Kubiak et al 1985*] with antimony as the n-type dopant. Although the preferred n-type dopant, antimony has a complex incorporation behaviour

due to a temperature dependent sticking coefficient and a tendency to surface accumulate. To produce good quality material, high growth temperatures >550°C are required. However, when using this temperature regime, antimony has a very low incorporation coefficient leading to the formation of a surface (accumulated) adlayer of Sb. Thus, when trying to produce a high/low doping transition, the profile is smeared due to the subsequent incorporation of the adlayer, which acts as a reserve of dopant even if the Sb cell has been shuttered. Using PED, a negative bias is applied to the substrate during Sb doping. This is thought to accelerate Si^+ ions produced by the Si e-beam evaporators, which breaks up the Sb adlayer leading to an enhancement of Sb incorporation of up to 10^3. This allows abrupt transitions in doping concentration by variation of the PED voltage.

The antimony DSL'S were designed to show if an enhanced mobility DSL was possible, with the design of the structures following the principles given in chapter 2.4. The layers were grown on p⁻ substrates, which had an in situ flux clean at 900°C. A 0.4μm boron doped buffer was grown at a growth temperature of 800°C with a growth rate of 0.27nm s^{-1}. Then using PED voltages of -800V and 0V, a doping level transition of $1x10^{18}cm^{-3}$ to an expected low doping of $1x10^{15}cm^{-3}$, formed the high/low doping profile in the superlattice. The wafer specifications are given in table 3.2, with a schematic of the designs in figure 3.2 .

TABLE 3.2

GROWTH PARAMETERS OF Sb DSL's

Wafer ID.	N_{high} /cm^{-3}	N_{low} /cm^{-3}	d_1 /nm	d_2/nm	No. of Periods	Substrate type
113.6	$1x10^{18}$	$1x10^{16}$	3	3	30.5	p-
112.12	$1x10^{18}$	$1x10^{16}$	3	10	30.5	p-
112.14	$1x10^{18}$	$1x10^{16}$	3	20	30.5	p-
112.10	$1x10^{18}$	$1x10^{16}$	3	40	30.5	p-

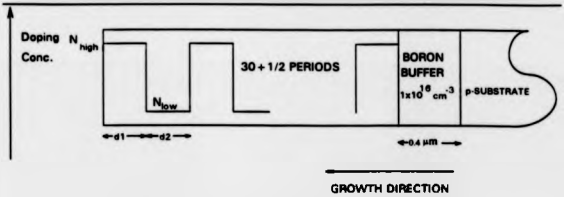


Figure 3.2 Schematic of antimony doping superlattice.

3.1.3 GROWTH OF "ULTRA-THIN" Sb DOPING LAYERS OF VARIABLE WIDTH

Ultra-thin doping layers "UTDL" with widths between 5 and 500nm, were grown on p- substrates, using the same growth rate and wafer preparation as the antimony DSL's (chapter 3.1.2). The antimony doped regions were grown at a constant growth rate, using PED to achieve the high doping level. The PED voltage was kept at zero volts during growth of the boron buffers, where a boron doping level of $5x10^{16}cm^{-3}$ used to compensate the incorporation of $1x10^{16}cm^{-3}$ antimony. The design specifications are given in table 3.3, with a design schematic shown in figure 3.3.

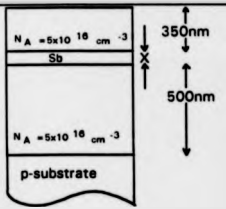


Figure 3.3 Schematic of "Ultra-Thin" Antimony doping wafer.

TABLE 3.3

UTDL'S LAYER SPECIFICATIONS

Wafer ID.	Doping Layer thickness(X) /nm
114.4	5
114.7	10
114.3	20
114.8	40
114.5	80
114.6	500

3.1.4 GROWTH OF BORON DELTA DOPED LAYERS

Similar growth processes were used for the production of boron delta doped layers for tunnelling spectroscopy studies and for δ-FET production.

For tunnelling studies, the layers were grown on 1-2 ohm cm n-substrates after a silicon flux clean at 850°C. 400nm of Si was deposited at a growth rate of 0.3 nms^{-1}, the temperature being continuously lowered from 760°C to 480°C during this stage of

growth. The silicon flux was then interrupted and the required boron concentration deposited. Finally, the boron cell was shuttered and growth of silicon was continued for a further 20nm at 480°C, the residual doping level in the epilayer was in the range 10^{14}-$10^{15}cm^{-3}$. The growth specifications are given in table 3.4.

TABLE 3.4

DESIGN PARAMETERS USED IN TUNNELLING SPECTROSCOPY LAYERS

Wafer ID	Cap / nm	Delta sheet Conc. N_s /cm^{-2}	Buffer / nm	substrate type
9.31	25	$1x10^{14}$	400	p-
116.15	20	$2x10^{13}$	400	n-

For the boron δ-FET, the wafers were grown on 1-2 ohm cm n⁻ substrates in a similar manner to those of used the boron δ tunnelling study. The cap and buffer layers were doped with antimony at $10^{18}cm^{-3}$. The as grown specification included an extra 22.5nm of silicon cap, which was consumed in the production of the gate oxide. The layer specifications are given in table 3.5, with a schematic of the wafer design in figure 3.4. Wafer 116.8 was used for SIMS analysis, so that a comparison could be made with SIMS analysis of wafers processed into δFET devices. Wafer 116.14 was an n⁺substrate, so that PMOS FET structures could be produced and compared with p-channel δ-FET devices.

3.1.5 GROWTH OF ANTIMONY δ-DOPED TUNNELLING LAYER

The antimony δ-doped tunnelling wafer was grown using the solid phase epitaxy technique. A p⁻(10-60 ohm cm) substrate was given a flux clean at 850°C, with growth at 600°C at a rate of 0.1nm/s to give a buffer thickness of 350nm. Growth was stopped, and the layer allowed to cool to room temperature. Antimony was then deposited to the required surface concentration. Growth was recommenced to produce a 25nm cap at a

growth rate of 0.05nm/s, leaving the antimony layer physically incorporated. Recrystallisation of the polycrystalline cap was then at 760°C. Wafer specifications are given in table 3.4.

TABLE 3.5

DESIGN SPECIFICATIONS OF δFET WAFERS

Wafer ID.	Cap as Grown /nm	Delta Sheet Concentration / cm^{-2}	Cap after Oxidation /nm
116.7	42.5	$1x10^{12}$	20
116.8	42.5	$1x10^{12}$	N/A
116.9	42.5	$5x10^{11}$	20
116.10	42.5	$2x10^{12}$	20
116.11	32.5	$1x10^{12}$	10
116.12	52.5	$1x10^{12}$	30
116.13	62.5	$1x10^{12}$	40
116.14	n- substrate	N/A	N/A

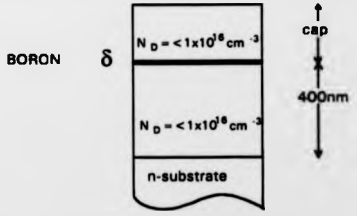


Figure 3.4 Schematic of boron δ-layers.

3.2 MEASUREMENT TECHNIQUES

3.2.1 HALL EFFECT MEASUREMENTS

One of the attractions of the Hall effect is the apparent simplicity of the measurement. The simple rectangular cross section bar used to derive the expressions for the Hall coefficient in chapter 2.5 is generally very difficult to produce. The most popular sample geometry was proposed by van der Pauw(1958), and various sample geometries are shown in figure 3.5. These sample shapes have the advantage over the conventional Hall bar of only requiring four contacts located on the periphery of a sample. This is especially useful for the rapid assessment of epitaxial material where an arbitrary shaped sample can be used. The van der Pauw technique requires that the sample is:

(a) homogenous and isotropic

(b) Uniform in thickness

(c) Four contacts are located on the periphery of the sample

(d) The contacts are infinitely small

An additional consideration for epitaxial layers is junction isolation of the epitaxial layer from the substrate. This is usually achieved by the use of a substrate which has the opposite conduction type compared with the epitaxial layer. For example, the Sb DSL's are grown on p-substrates.

For a current passed through contacts A and B (figure 3.6), a voltage V_{CD} appears across contacts C and D. If the contacts are commutated so that BC are the current electrodes and AD are the potential probes, then van der Pauw showed that the resistivity (ρ) is given by ;

$$f(\rho) = \exp\left(\frac{-\pi d R_{AB,CD}}{\rho}\right) + \exp\left(\frac{-\pi d R_{BC,DA}}{\rho}\right) - 1 = 0 \qquad (3.1)$$

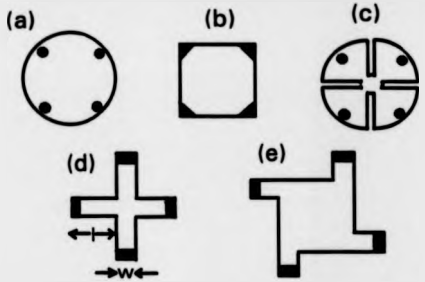


Figure 3.5 Possible sample shapes for Van der Pauw measurements. (a) circle, (b) square, (c) clover leaf, (d) Greek cross, (e) Pin-wheel.

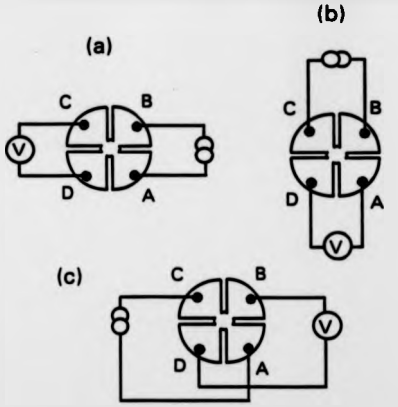


Figure 3.6 (a,b) Van der Pauw resistivity measurement configuration. (c) VDP Hall measurement configuration for a magnetic field perpendicular to the sample.

If the contacts are along orthogonal diameters of a circular specimen then $R_{AB,CD} = R_{BC,DA} = R$ and the resistivity can be determined from one measurement, and equation (3.1) gives;

$$\rho = \frac{\pi d R}{\ln 2} \tag{3.2}$$

where d = thickness of the sample.

A general solution to equation (3.1) is given by;

$$\rho = \left(\frac{\pi d}{\ln 2}\right)\left(\frac{R_A + R_B}{2}\right) f\left(\frac{R_A}{R_B}\right) \tag{3.3}$$

where $f(R_A/R_B)$ is a dimensionless quantity dependent only on the ratio of R_A and R_B. $f(R_A/R_B)$ can be evaluated from;

$$\frac{(R_A - R_B)}{(R_A + R_B)} = \frac{f}{\ln 2}\cosh\left(\frac{\exp\left(\ln 2 / f\right)}{2}\right)^{-1} \tag{3.4}$$

For $R_A \geq 10\% R_B$ then Van der Pauw gave an approximate solution for $f(R_A/R_B)$ as;

$$f\left(\frac{R_A}{R_B}\right) = 1 - \left[\frac{R_A - R_B}{R_A + R_B}\right]^2 \frac{\ln 2}{2} - \left[\frac{R_A - R_B}{R_A + R_B}\right]^4 \left[\frac{(\ln 2)^2}{4} - \frac{(\ln 2)^3}{12}\right] \tag{3.5}$$

Errors in the determination of the resistivity and Hall coefficient produced by finite sized contacts have been studied for the van der Pauw geometries shown in figure 3.1a,b by Chang *et al* (1974) and Koon *et al* (1989). Van der Pauw proposed the clover leaf design to reduce contact placement errors, with the Greek cross pattern regarded as an extreme example of the clover leaf. The theoretical errors introduced by using a Greek cross pattern have been studied by Versel(1979) and David *et al* (1977). For geometries where $l/w > 1$ (figure 3.5d), then contact shorting effects

due to this structure can be neglected, and the error introduced into the sheet resistance is 0.1%. The Pin-wheel and Greek cross structures(fig. 3.5d,e) are frequently incorporated as diagnostic test structures in microfabrication processes, and are used for example to determine the uniformity of an implant, diffusion etc. Such samples with lithography limited symmetry may easily have a van der Pauw correction factor close to 1 (i.e. $f(R_A/R_B)=1$). The cross also allows the use of large area contacts that are well spaced from the active area of the device. De Mey(1973) also showed that the cross geometry also produced the lowest Hall voltage error.

Buehler *et al* (1978) investigated various size cross structures, produced using a lithography technique. The results indicated that active areas of $6.4\mu m^2$ gave negligible error in the determination of the sheet resistivity, when compared to larger active areas, if the sample currents less than 1mA were used.

3.2.2 SYSTEMATIC ERRORS

Errors due to the noise of measured voltages and the calibration of magnetic field and current values limit the accuracy of the measured Hall coefficient. Hall effect measurements are also subject to various systematic errors which are a function of the galvanomagnetic voltages measured. If the sample measured has a longitudinal temperature gradient ΔT_x, then a transverse voltage V_N appears through the Ettingshausen-Nernst effect, and a transverse temperature gradient ΔT_y is set up by the Righi-Leduc effect. The latter generates a thermoelectric voltage between the Hall probes, for dissimilar sample and contact materials. Both the Righi-Leduc and the Ettingshausen-Nernst effects can be virtually eliminated by thermal anchoring of the sample and sample leads. The Ettingshausen effect is an inherent function of electron flow in a magnetic field, and the transverse temperature gradient is always present in usual experimental conditions. Minimisation of this effect is achieved by reducing the

sources of thermoelectric voltages. Use of an alternating sample current can reduce the errors if the period of the Hall voltage is short in comparison to the time required to set up the temperature gradients.

Although it is not possible to eliminate all the thermomagnetic effects, most can be eliminated by permutations of the current and magnetic field polarity. If V_h is the true hall voltage, V_c the misalignment, V_e the Ettingshausen, V_r the Righi-Leduc, V_n the Nenst-Ettingshausen and V_T the thermoelectric error voltages introduced by a thermal gradient across the sample. Then for the current(I) and magnetic field(B) polarities given below, V_h can be extracted.

$$
\begin{aligned}
B+,I+ &= +V_h + V_e + V_r + V_T + V_n + V_c \\
B-,I+ &= -V_h + V_e - V_r + V_T - V_n - V_c \\
B+,I- &= -V_h - V_e - V_r + V_T + V_n + V_c \\
B-,I- &= +V_h - V_e + V_r + V_T - V_n - V_c
\end{aligned}
$$

rearranging the above equations gives;

$$
\frac{1}{4}\left(V_{(B+,I+)} + V_{(B-,I-)} - V_{(B-,I+)} - V_{(B+,I-)}\right) = V_h + V_e = V_h + P\Theta \qquad (3.6)
$$

where P is the Ettingshausen coefficient and Θ is the Seebeck coefficient.

Using the van der Pauw sample geometry, the Hall voltage is determined from the voltage measured across **BD** for a current passed through **CA**(figure 3.6b) for a magnetic field applied perpendicular to the sample. Then using the above permutations of field and current the average Hall voltage is obtained (Similarly the Hall voltage $V_{BD,CA}$ is obtained). The Hall coefficient (R_h) in cm^3/C is given by;

$$
R_h = \frac{10^8 V_h d}{BI} \qquad (3.7)
$$

where B = field measured (gauss)

I = sample current (Amps)

d = sample thickness (cm)

The sign of R_h determines then sign of the charge carriers. The units of equation (3.7) are those encountered in practice, although they are not SI units. A conversion is given in the ASTMS standards(1975).

For a single type of charge carrier the Hall coefficient is related to the carrier concentration by:

$$R_h = \frac{r}{nq} \tag{3.8}$$

where n is the carrier concentration, q is the charge of the carriers and r the Hall scattering factor, which is taken as equal to 1 (see chapter 2.5).

The Van der Pauw geometry although suitable for most material assessment is not ideal for magnetoresistance measurements due to the difficulty in distinguishing between the "physical" and "geometrical" contributions. In addition, it is difficult to separate the contributions that ρ_{xx} and ρ_{xy} make to the conductivity tensor in the presence of a high magnetic field. Thus for high field measurements the Hall bar (also called the Hall bridge) geometry is preferred, with a length to width ratio chosen to reduce the geometrical magnetoresistance contribution.

3.3 HALL EFFECT MEASUREMENT SYSTEMS.

3.3.1 4-300K (0.5T) MEASUREMENT APPARATUS

The requirement to measure the Hall coefficient as a function of temperature has led the author to design and build a DC Hall measurement system using the Van der Pauw sample configuration. The system is based around a liquid helium bath cryostat and an electromagnet. The system is partly automated and control of the measuring instrumentation is via a BBC master computer and Procyon IEEE interface. Control

software has been written by the author, where all measurement variables are calculated and displayed, and the data stored onto disk with a hardcopy output as back-up. The measurement system has been improved over a period of time and the following sections give a resume' of its final configuration. An overview of the major components of the Hall measuring system is given in figure 3.7.

3.3.2 4K CRYOSTAT

For Hall measurements in the temperature range 4-300K, a Thor bath cryostat shown in figure 3.8 has been used. The cryostat consists of a vacuum and superinsulated helium reservoir shielded by means of a gas cooled radiation shield. Variable temperature operation of the sample is affected by conduction/convection in a helium exchange gas column, with a heater element attached to a copper block. Electrical connections to the sample were via PTFE sleeved copper wires. Access to the sample was via a removable and rotatable seal, which allowed the sample to be orientated within the magnetic field. The cryostat was mounted within an alloy frame, with the tail piece, which contains the sample holder, centrally located between the pole pieces of a "Newport", 4" electromagnet. A diffusion pump vacuum system allowed evacuation of the isolation jackets and enabled the pressures of the exchange gas and sample gas to be varied. The sample holder was constructed from "Tufnol", to provide electrical isolation $> 10^{10}\Omega$, with phosphor bronze contact springs to attach samples. Figure 3.9 shows a schematic of the sample holder, with an epitaxial Van der Pauw sample attached. Samples up to $10 \times 10 mm^2$ could be mounted.

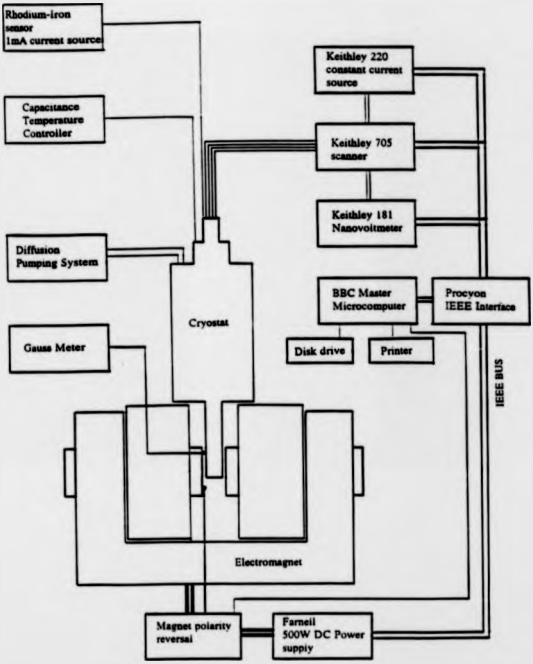


Figure 3.7 Schematic of Van der Pauw measuring system.

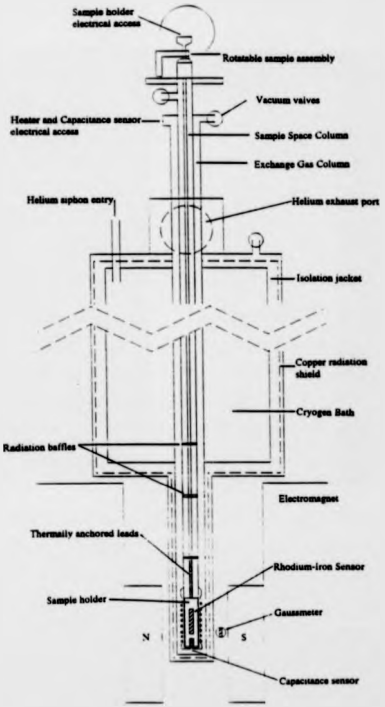


Figure 3.8 Schematic of bath cryostat.

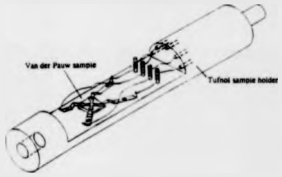


Figure 3.9 Schematic of Hall sample holder used in bath cryostat.

3.3.3 TEMPERATURE MEASUREMENT AND CONTROL

Variable temperature operation of the cryostat was achieved by use of a Lake Shore Cryotronics cryogenic capacitance temperature controller. A strontium-titanate($SrTiO_3$) glass ceramic sensor was mounted on the exchange gas column heater block (fig. 3.8) and provides a single value output between 1K and 60K and from 60K to 300K. The sensor is unique in having $<0.05\%$ magnetic field dependence in fields up to 15T, which makes its application in a Hall measuring system particularly useful. A ten watt heater element constructed from constantan wire, was non-inductively wound around the copper heater block at the end of the exchange gas column; details are shown in figure 3.8

Although the capacitance sensor is ideal for temperature control, it has a non-reproducible temperature dependence making it unsuitable for temperature measurement. Therefore, a rhodium-iron sensor with a reproducibility of 0.01K was used for temperature measurement. Using a 1mA excitation current gives a sensitivity of 0.01K per microvolt. Voltage measurement was by a Keithley 181 nanovoltmeter, allowing temperature measurement to ±0.01K. The RhFe sensor gives an error of 10% in a magnetic field of 2.5T[Oxford Instruments]. However, the operation of the cryostat

utilises the capacitance sensor for temperature control, and the RhFe sensor for temperature measurement only when the magnetic field was at zero. The RhFe sensor was secured to the reverse side of the sample holder (figure 3.9), by apezion N grease and mylar straps. The sensor leads and sample measurement leads were thermally anchored to the sample rod assembly.

3.3.4 VOLTAGE AND CURRENT SWITCHING

The current and voltage switching required by the Van der Pauw technique was achieved through the use of a Keithley 705 IEEE programmable scanner. Voltage switching (between sample and voltmeter), was by a 7059 low voltage card, with a differential input isolation of $>10^9$ ohms and noise of $<1\mu V$. For current switching, a 7056 general purpose card with an isolation of $>10^9$ ohms was used. The cards each contain 10 DPDT relays and twelve are used to provide the necessary switching.

Sample currents were supplied from a Keithley 220 programmable constant current source which could output currents between 100mA to 1nA. Voltages were measured by a Keithley 181 nanovoltmeter. On the lowest range (2mV), the nanovoltmeter has a noise figure of 30nV p-p, and an input resistance of $>1G\Omega$. Although the K181 was non-autoranging, the Hall software adjusted the sensitivity of the meter via the IEEE bus to give the most accurate voltage reading. (A block diagram of the apparatus used is given in figure 3.7)

For sample resistances $>100K$, the output bias current on the K181, which was dependent on the range of the meter and the sample resistance, gave erroneous voltage measurements. This effect was minimised by buffering the inputs of the K181 with two unity gain 7650 amplifiers. These buffers have an input bias current of 10pA and an input resistance of 10^{12} ohms. Introduction of the buffers increased the noise to $2\mu V$ pk-pk.

3.3.5 MAGNETIC FIELD CONTROL

The "Newport" electromagnet used to provide the magnetic field, could achieve a field of 0.55T with a current of 7.5Amps supplied from an IEEE programmable Farnell AP500 DC power supply. Typical Hall measurement conditions used a magnetic field of 0.4T, with the field monitored by a Gauss meter. To eliminate the galvanomagnetic errors described in 3.2.2, the sample was rotated by 180°.

The final configuration of the apparatus enable the polarity of the field to be reversed via the action of an external DPDT 20A relay actuated by a signal sent from the BBC through the 8 bit user port. The signal was opto-isolated and amplified to give a voltage swing of 5V. To prevent the reversing relay becoming open circuit during magnet operation, protection circuitry was provided via two Hall effect I.C sensors mounted on the pole pieces of the electromagnet and a logic board designed by the author (figure 3.10). Operation in this configuration required further diagnostic checks on the stability of the acquired data, to eliminate the eddy current heating effects on the cryostat tail assembly.

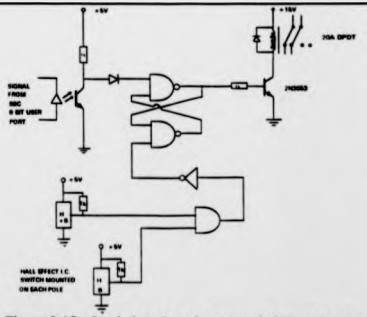


Figure 3.10 Logic board used to control electromagnet.

3.4. 0.3K CRYOMAGNETIC SYSTEM

Low temperature measurements were made in a Oxford Instruments cryomagnetic system. This was composed of a helium-3 closed cycle system inserted within a superconducting solenoid, mounted to give a vertical magnetic field of up to 12 Tesla at 4.2K. The insert had a base temperature of 0.3K and a hold time at this temperature of approximately 1.5 hours. A top loading probe enabled the sample to be lowered directly into the insert, without losing the helium-3.

Temperature measurement was via a Ge resistor in the range 0.3K to 4K, and a Si diode between 4K and 300K. The accuracy of the temperature calibration was $\pm 0{\cdot}75$mK below 4K for the Ge resistor and ± 30mK for the Si diode.

Temperature control was by an Oxford instruments ITC4 temperature controller, using Speer resistors. Although these resistors have a low magnetic field dependence(6% at 12T), magnetoresistance measurements at temperatures other than that of the 1K pot(1.4K) or the base temperature(0.3K), were made by using the capacitance sensor and temperature controller, described in section 3.3.3.

3.4.1 0.3K, 12 TESLA HALL MEASUREMENTS

Measurements of the Hall coefficient and magnetoresistance at very low temperatures (0.3K) requires sample heating to be minimised. This has been achieved in the present work by using an alternating sample current of $< 10^{-7}$A, combined with lock in and phase detection techniques and a d.c magnetic field. Furthermore:

(i) If the period of the Hall voltage is short compared to the time required to set up a temperature gradient in the sample, then Ettingshausen voltage can be reduced.

(ii) The use of a lock-in amplifier increases the ultimate sensitivity for measurement of Hall voltages on low resistance samples, enabling voltages of $< 1\mu V$ to be easily detected.

The measurement system was based around an EG&G 5209 lock-in amplifier (LIA). This provided an oscillator output, phase sensitive detection, filtering and amplification in one unit. The measurement circuit is shown if figure 3.11. Typically a 1V pk-pk sinusoidal voltage(V_s) was connected in across current source resistor (R_s), a current sense resistor (r_s) and the sample resistance R_{xx}. If $R_s > r_s > R_{xx}$ then the current through the sample is determined by the value of R_s, and is approximately constant. Typical experimental values of, $r_s = 1k\Omega$, $R_s = 10M\Omega$, and an oscillator frequency of 13Hz were used.

The resistivity(ρ) in ohm metres of the bridge sample (equ. 3.9) was determined from the average of the voltages across the V_{35} and V_{46} voltage probes (figure 3.11).

$$\rho = \frac{1}{2}(V_{35} + V_{46})\frac{wt}{IL} \qquad (3.9)$$

where w = sample width (m)
L = distance between voltage probes (m)
t = sample thickness (m)
I = sample current (A)

Similarly the Hall voltage was determined across the V_{34} and V_{56} voltage probes with a reversal in the magnetic field.

The experimental procedure for magnetoresistance measurements was as follows. The temperature of the sample was first set. A sample resistance measurement was obtained and the sample current monitored. The magnetic field was then ramped slowly to a set point. A repeat measurement of the magnetoresistance was only obtained when the temperature had restabilised. The process was then repeated for as many times as required. After powering down the magnet, the temperature had only drifted by ±2mK. Measurements were then repeated for the opposite field direction.

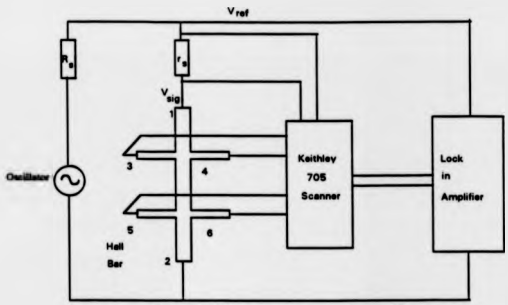


Figure 3.11 A.C Hall measurement configuration.

3.5 ELECTROCHEMICAL CAPACITANCE VOLTAGE PROFILING

Capacitance voltage (CV) measurements are frequently used for process monitoring on MOS devices and are routinely used to measure implant profiles and oxide contamination. The technique relies on the depletion approximation for a one sided abrupt junction (metal-n or p^+-n), where the depletion width (x_d) for a reversed biased Schottky barrier is given by:

$$x_d = \left(\frac{2\varepsilon\varepsilon_r (V_b + V_a)}{qN_d} \right)^{\frac{1}{2}} \qquad (3.10)$$

where V_b is the barrier height, V_a the external reverse bias and N_d the donor doping concentration. For a doping concentration N_d independent of distance x, the charge Q stored in the depletion region of width x_d is given by:

$$Q = A(2\varepsilon\varepsilon_s qN_d(V_a + V_b))^{1/2} \tag{3.11}$$

For a small change in bias ΔV_a, the depletion width will increase causing a charge increase ΔQ. Thus the small signal capacitance associated with the depletion region is given by:

$$C_s = \frac{dQ}{dV_a} = \frac{1}{2}A\left(\frac{2\varepsilon\varepsilon_s qN_d}{(V_a + V_b)}\right)^{1/2} = \frac{\varepsilon\varepsilon_s A}{x_d} \tag{3.12}$$

The above expression is exactly the same formula for the capacitance of a parallel plate capacitor. Therefore from a measurement of the capacitance, N_d can be determined from equation 3.10.

For non-uniform doping the use of equation 3.10 to determine $N_d(x)$ is invalid. For a bias voltage V_a, the total voltage drop across the depletion region can be obtained from Poisson's equation:

$$(V_a + V_b) = \frac{1}{\varepsilon\varepsilon_s}\int_0^{x_d} x\rho(x)dx \tag{3.13}$$

where $\rho(x)$ is the space charge density (equal to $qN_a(x)$ for p-type material and $qN_d(x)$ for n-type material). If the bias is changed by ΔV_a, the depletion width changes by Δx_d and in the differential limit of equation 3.13, assuming V_b is constant, gives:

$$\Delta V_a = \frac{1}{\varepsilon\varepsilon_s} qx_d N(x_d)\Delta x_d \tag{3.14}$$

and the charge increment is:

$$\Delta Q(x_d) = qN(x_d)\Delta x_d A \tag{3.15}$$

The small signal capacitance is then given by:

$$\frac{\Delta Q(x_d)}{\Delta V_a} = C_s = \frac{\varepsilon\varepsilon_s A}{x_d} \tag{3.16}$$

Thus the small signal capacitance is given by the parallel plate capacitor expression for non-uniform doping within the depletion region. This result is needed to determine the depletion width from a measurement of the capacitance. Blood(1986) has then shown that the carrier density profile $N(x_d)$ can be determined from:

$$N(x_d) = \frac{-C_s^3}{\varepsilon\varepsilon_r qA^2}\left(\frac{\Delta C_s}{\Delta V}\right)^{-1} \qquad (3.17)$$

Typically the small signal capacitance C_s is measured as a function of the applied bias V_a, and the rate of change of C_s with V_a calculated, allowing the doping concentration $N(x_d)$ at the depth x_d to be determined from equation 3.17.

The maximum depth that can be profiled using conventional CV technique is limited by the onset of avalanche electrical breakdown, which corresponds to a maximum electric field of $\cong 4 \times 10^5 Vcm^{-1}$. This limits the maximum depth to $\cong 0.02\mu m$ for material doped at $N_d = 10^{18} cm^{-3}$, which corresponds to 2×10^{12} charges per cm^{-2}. This ignores the difficulty of producing a practical Schottky barrier on highly doped material, with a low reverse bias current. Both of these restrictions are removed if an electrolyte is used to form the Schottky barrier, with anodic dissolution of the silicon using the same electrolyte. A fixed value of the Schottky bias voltage is then used to determine the carrier concentration, after a known amount of silicon has been removed from the surface. The material removed (x_e) can be calculated by integrating the dissolution current and using Faraday's law of electrolysis.

$$x_e = \frac{M}{ZFDA}\int Idt \qquad (3.18)$$

where A = junction area

F = Faraday's number

Z = dissolution valency

D = density of the semiconductor

M = molecular weight of the semiconductor

The total depth for a capacitance measurement is then given by $x_d + x_e$.

A commercial instrument, the Bio-Rad PN4200 electrochemical profiler was used in this work for electrochemical profiling of doping structures. The measurement principles used by the PN4200 were originally developed by Ambridge (1975). The depletion capacitance is measured by detection of the out of phase current signal arising from a signal of $0.1V_{pk\text{-}pk}$ at 1kHz. A second superimposed signal of $0.28V_{pk\text{-}pk}$ at 30Hz modulates the depletion width, from which dC_d/dV is obtained.

3.6 TUNNELLING SPECTROSCOPY

As discussed in chapter 2.3, fine structure in the current voltage characteristic of a metal-silicon-delta layer diode can provide information on the 2D density associated with the quantum well formed in the delta layer. Previous experimental methods have used an AC modulation technique [*Adler 1966*], where a swept DC bias voltage V_d, with a constant sinusoidal modulation voltage $\Delta V\cos\omega t$ is superimposed onto the sample. The resultant spectrum has the form;

$$I = I_o + \left(\frac{dI}{dV}\right)\Delta V\cos\omega t + \frac{1}{2}\left(\frac{d^2I}{dV^2}\right)\Delta V^2\cos^2\omega t \qquad (3.19)$$

Which can be expanded to;

$$I = I_o + \left(\frac{dI}{dV}\right)\Delta V\cos\omega t + \frac{1}{4}\left(\frac{d^2I}{dV^2}\right)\Delta V^2(1+\cos(2\omega t)) \qquad (3.20)$$

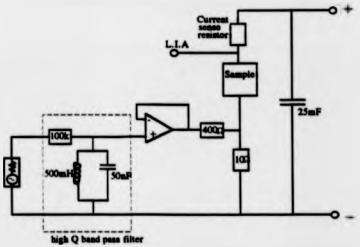


Figure 3.12 Circuit to determine dI/dV and d^2I/dV^2.

Thus detection at a frequency ω and 2ω gives a signal proportional to dI/dV and d^2I/dV^2. An attempt to use an AC method to determine dI/dV and d^2V/dV^2 was tried using the circuit given in figure 3.12. A dummy sample as used by Edgar *et al* (1985) was measured and gave comparable results. However the measurements of using this technique required a long time constant on the lock in amplifier. A faster experimental procedure was devised by Eisele(1989), where the current voltage characteristics were obtained using an HP4145B Semiconductor parameter analyser. This method was subsequently adopted by the present author for tunnelling spectroscopy measurements on the δ layer structures given in table 3.4. The current passed through the sample was averaged over 260 measurements to increase the signal to noise ratio. Using the built-in microprocessor, the values of dI/dV and (dI/dV)(I/V) were calculated. With the measurements taken at a constant DC bias, capacitive effects due to the Schottky barrier were reduced. The samples were mounted on to a PTFE sample holder with spring contacts of phosphor bronze. The experimental configuration for tunnelling measurements is shown in figure 3.13. A gold leaf was placed on each contact pad to prevent damage and lowered directly into a dewar of liquid helium.

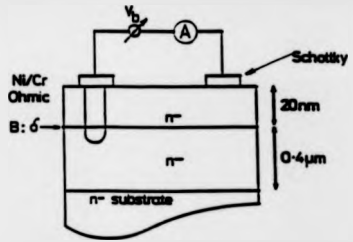


Figure 3.13 Schematic sample arrangement for tunnelling spectroscopy measurements of δ layers.

3.7 CONTACTS

The following sections describe the various sample preperations used in this work. One of the most difficult experimental techniques required for measuring the electrical properties of a semiconductor is the preparation of suitable contacts. For Hall measurements an ohmic contact, where the voltage drop due to the contacts is negligible compared to the resistance of the semiconductor, is required. For capacitance-voltage profiling, a reversed biased Schottky contact is used to modulate the depletion width in a semiconductor.

The basic principles of contact formation can be described by looking at the energy profile of an n-type semiconductor and metal. In figure 3.14a, the metal and semiconductor are separated, where Φ_m is the thermionic work function of the metal and χ is the electron affinity of the semiconductor measured from the bottom of the conduction band to the vacuum level. Thermal equilibrium is established (figure 3.14.b, where V_b is the diffusion potential) after intimate contact has been made between the metal and the semiconductor.

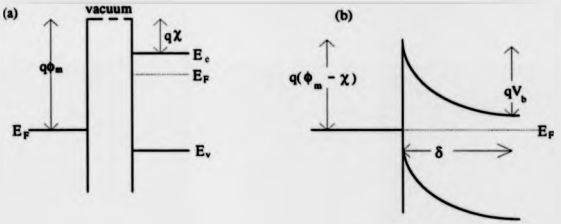


Figure 3.14 Formation of a metal-semiconductor contact. (a) before contact, (b) after thermal equilibrium.

Charge flows from the semiconductor to the metal, and allows the Fermi levels to align. The Fermi level in the semiconductor falls by an amount equal to the difference in the work functions. To preserve charge neutrality, negative charges are induced on the metal surface and an equal but opposite charge is induced on the semiconductor, with free carriers depleted from a length δ.

The barrier height (ϕ_B) is then given by;

$$q\phi_{Bn} = q(\phi_m - \chi) \qquad \text{for n-type} \qquad (3.21)$$

$$q\phi_{Bp} = E_g - q(\phi_m - \chi) \qquad \text{p-type} \qquad (3.22)$$

The barrier height depends only on the thermionic work function of the metal and the electron affinity of the semiconductor. However, the equations (3.21) and (3.22) neglect the role of surface states. The action of these is to pin the Fermi level and hence the barrier height becomes dependent only on the doping and surface properties of the semiconductor.

The specific contact resistance R_c (ohm cm^2) is defined as $R_c = (dV/dJ)$; where R_c is determined from the current density(J) and voltage characteristics(V). For highly doped material, e.g. $N_d > 10^{19} cm^{-3}$, R_c is dominated by tunnelling through the barrier, and $R_c \propto \exp(\phi_B/\sqrt{N_D})$. With low doped material, R_c is independent of N_d and thermionic emission through the barrier dominates. Thus to produce an ohmic contact a low barrier height is required. This is easier to achieve with p-type material (*Sze ch5 1981*). An alternative technique requires the contact area to be selectively doped, so that a thin tunnelling barrier is produced.

3.7.1 IN-HOUSE HALL SAMPLE PREPARATION

Epitaxial samples of the required van der Pauw geometry, suitable for inserting into the Hall system described earlier (chapter 3.2), were obtained by cleaving a $8x8mm^2$ section from the wafer. Although this shape is suitable for quick diagnostic measurements, a mesa etched Greek cross geometry is preferred. The experimental procedure was as follows;

(i) the sample was cleaned in propan-2-ol and then blown dry with $He_{(g)}$, to remove silicon dust.

(ii) A cross shaped mask of "Apezion W" wax, dissolved in xylene, was painted onto the epitaxial surface.

(iii) A silicon etch of CP_4A ($5HNO_3$:3HF:3Acetic acid) for 30s, removed any silicon not masked by the wax.

(iv) The etched sample was then rinsed in DI water, and then placed in fresh xylene to dissolve the mask. This left a cross shaped sample standing proud of the substrate. Finally the sample was rinsed in DI water and dried with $He_{(g)}$.

3.7.2 PRACTICAL OHMIC CONTACTS

For measurements in the temperature range 77-300K on moderately doped material, GaIn eutectic made suitable ohmic contacts. The contact pads were first cleaned of the native oxide with a 5% solution of HF. The GaIn was then applied with a piece of indium to the contact pad, and a piece of gold foil finally placed on top. The sample was then held in the sample holder with phosphor bronze springs and the ohmicity of the contacts checked with a curve tracer. Junction isolation of the epilayer from the substrate was also checked at this stage.

For low temperature measurements a different contacting procedure was used, as GaIn contacts tended to become non-ohmic for temperatures less than 77K. Aluminium is the preferred contacting material for silicon, given its variation in barrier height with sintering temperature. Aluminium (1% Silicon) was sputtered through a patterned stainless steel mask, to leave four $1mm^2$ pads. The appropriate sintering temperature is dependent on the doping and type of the silicon, and is typically $< 420^oC$ for n-type, and $> 450^oC$ for p-type material in an $N_{2(g)}$ atmosphere. Sample preparation then followed as in chapter 3.7.1. For low doped n-type material AuSb was evaporated from a tantalum boat in a bell jar vacuum system. The samples were then annealed at 380^oC in $N_{2(g)}$.

3.7.3 DOPING SUPERLATTICES

For the doping superlattice study two contacting procedures have been used. To investigate the work of Nagagawa(1986), a contact that connected to as many layers of

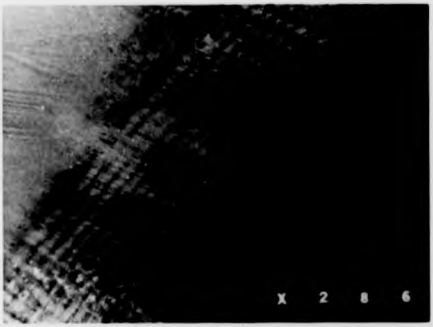


Figure 3.15 Optical microscope photograph of stained boron doping superlattice. The sample has been bevelled to expose the structure.

a superlattice as possible was desirable, with the constraint of also requiring to keep junction isolation so that a spurious parallel conduction path in the substrate would not be made. The boron superlattice samples were bevelled to expose the superlattice layers. Using a copper stain the layers were capable of being resolved under a microscope, figure 3.15. A metal mask was placed over the exposed layers and aluminium evaporated to form the contact regions. Annealling above the Al-Si eutectic temperature of 580°C provided a blocking contact to the substrate. The final sample configuration is shown in figure 3.16.

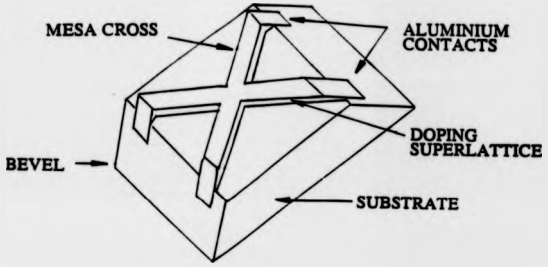


Figure 3.16 Schematic of Van der Pauw sample used for measurements on boron doping superlattice.

Although suitable samples were fabricated, bevelling tended to produce a high failure rate in sample production. Therefore a second method of fabrication, using microfabricated samples with ion implanted contact regions was used for the study of Si:Sb DSL's.

3.7.4 DELTA LAYERS

For Hall measurements on highly doped δ layers $>1x10^{14}cm^{-2}$, GaIn eutectic has been used successfully by Mattey(1991). A short tunnelling barrier is created giving an almost ohmic contact. However, this measurement is only reliable at 4K when all parallel conducting channels have been frozen out. For lower doped layers, sputtered NiCr was used [*Eisele 1989*], to provide an ohmic contact to the delta layer via a tunnelling process, whilst producing a blocking contact to the low doped buffer layers. This method of fabrication has been used by the author, where NiCr has been sputtered through a stainless steel mask and a van der Pauw structure as described in section 3.7.1 has then been fabricated. Annealing of the contacts was performed at 460°C for 10-20minutes in an N_2 ambient.

3.7.5 TUNNELLING SPECTROSCOPY DELTA LAYERS

Sputtered NiCr, annealed at 460°C, forms the ohmic contact to the δ layer samples. For the antimony delta layer sample, a Schottky contact was produced by evaporating AuSb from a tantalum boat, through a metal mask to leave a $1mm^2$ area contact. No further heat treatment was used.

For the boron δ layer sample, sputtered Al-Si(1%) was tried as a Schottky barrier. Although the barrier height is predicted to be 0.5eV[*Smith 1971, Card 1975*], the contacts produced were ohmic to the delta layer. Reducing the sputtering time of the Al and rotating the sample within the Al plasma produced unreliable contacts. The

final sample configuration used GaIn eutectic to form the Schottky barrier on the untreated surface of the sample, the native oxide being intended to act as a diffusion barrier. Samples produced using this method, were then inserted into the liquid He soon after fabrication to prevent diffusion of the GaIn.

3.7.6 E-CV SAMPLE PREPARATION

A cleaved sample of 100mm^2 was placed onto the electrolyte sealing ring of the Bio-rad PN4200 e-CV sample holder. GaIn eutectic was then used to make an ohmic contact to the sample, with a solution of 1M NaF and 0.05M H_2SO_4 forming the electrolyte Schottky barrier. This method has been shown to give good quantitative profiles of submicron doping structures (*Leong et al 1985a, Biswas et al 1988*).

Experimental profiling conditions were then determined from diagnostic IV, $(1/C^2)/V$ and GV curves. The choice of the bias voltage is the most important, as a small leakage current through the Schottky barrier is required and a continuos value of $(1/C^2)/V$. Further experimental details are given in the thesis of Leong(1985b).

3.8 SAMPLE FABRICATION AT THE EDINBURGH MICROFABRICATION FACILITY

3.8.1 MICROFABRICATED HALL SAMPLES

The use of in-house processing techniques allows the fast acquisition of material parameters such as layer type, concentration and mobility. However, for low temperature measurements, reliable and reproducible contacts are required. For measurements on the Si:Sb doping superlattices and Ultra thin doping spikes of variable width, contacts with a known depth are especially important where isolation of active layer from the substrate is required to avoid spurious results. The use of ion implanted

contacts is especially useful for measurements on buried layers, for example in δ layers, where isolation of buffer layers is performed by using opposite polarity implanted contacts.

A modified CMOS processing schedule (Edinburgh Microfabrication Facility) has been used to fabricate Hall bridge and van der Pauw structures. As the use of high temperatures is precluded, deposited pyrolytic oxide has been used for passivation and as a barrier against the reactive ion etch (RIE) steps. Deposition of pyrolytic oxide is performed at 430°C which is below the doping growth temperatures used in this study. A typical process sequence is as follows;

Mask 1: Trench etch to provides a mesa structure.

Mask 2: Implant 1 to provide ohmic contact to active layer.

Mask 3: Implant 2 to provide ohmic contact to substrate.

Mask 4: Open contact windows in pyrolytic oxide.

Mask 5: Metallisation (Al)

A 3x3mm^2 die size was utilised, with alternate rows and columns left blank for further characterisation. The use of lithography allows the geometrical limitations of the various Hall structures to be reduced. The Hall structures on mask set Eu718 were designed using the ASTMs standards, and included a Van der Pauw structure where $l/w > 3$ (figure 3.17) and a Hall Bar where $l/w > 10$. Further details of mask production and design can be found in the thesis of Smith(1993).

On receiving processed wafers, ohmic contacts were tested using a MP1000W probe station and HP4145B parametric analyser. No problems were found with non-ohmic contacts. Suitable chips were then removed, identified, and cemented into ceramic headers using silver loaded epoxy. The chips were cured and then gold wire bonded using a Kulika & Soffa thermosonic ball wedge bonder. This sample preparation gave reliable ohmic contacts that could be repeatedly temperature cycled. Enamelled copper wires were then soldered to the pins, and the wired chips mounted into the measuring apparatus.

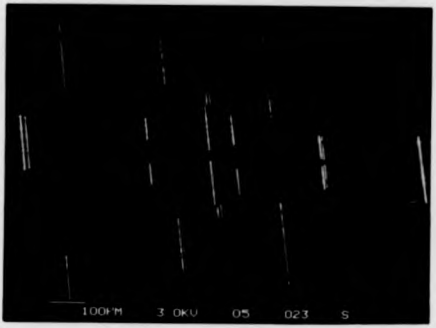


Figure 3.17 Microfabricated Van der Pauw sample.(l/w > 3).

3.9 DELTA-FET DEVICE PRODUCTION

3.9.1 DELTA-FET FABRICATION PROBLEMS

The fabrication of a δ-FET has several unique processing problems which prevents the use of a typical MOS processing schedule. The first concerns the thermal budget allowance for each wafer. With typical boron delta layer growth at 480°C, an ideal thermal budget allowance for each wafer should not exceed those used in wafer production.

There are typically two high temperature areas in conventional processing. First is the high temperature required for thermal oxidation of silicon to produce a gate dielectric, typically 750-1200°C for 30 minutes. Second, is the high temperature required for implant activation. Experimental evidence for the diffusion of boron delta profiles is given in the work of Powell(1991b), which suggests that a low temperature anneal of 700°c for 1 hour produces broadening of 4nm. However, this is not suitable for an activation anneal. An anneal performed by the author on a boron delta layer for 30s @ 975°C (figure 3.18) produced no discernible broadening, within the error of the SIMS depth calibration.

Previous efforts to process MBE grown silicon [*Smith 1988*] involved a low temperature pyrolytic oxide for surface passivation and as a mask for the reactive ion etching. This oxide though was not of sufficient quality to be used as a gate oxide. Deposition of pyrolytic oxide involves silane and oxygen at atmospheric pressure. This is further doped with phosphorus so that a complex is formed with any Na contamination. The phosphorus interacts with interface charges, thus causing a threshold voltage shift. Deposition of pyrolytic oxide without phosphorus produces a low density oxide, and thus unstable devices. The requirement for a good low thermal budget oxide was satisfied through the use of a low temperature plasma enhanced

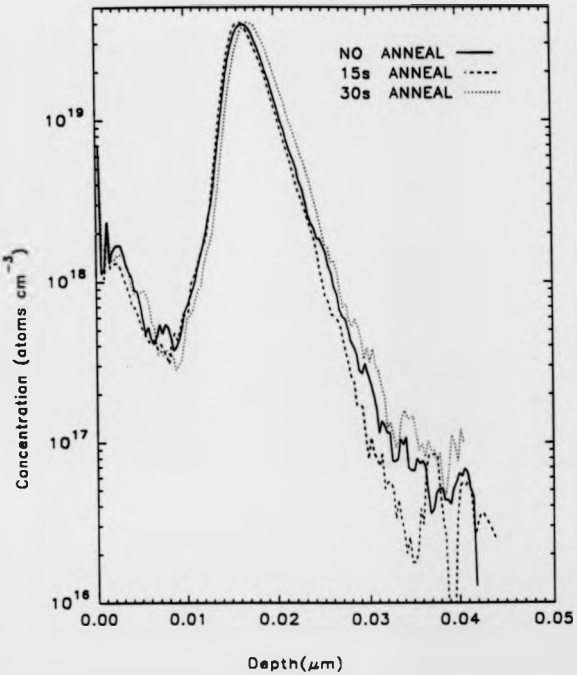


Figure 3.18 SIMS profile of a boron delta layer annealed at 975°C for 15 and 30 seconds. (Profiling conditions of 2keV O_2^+ normal incidence.)

oxidation process [*Taylor et al 1987,88*]. The advantages of this method of oxide production include anisotropic oxidation, fewer oxidation enhanced defects such as silicon stacking faults and lower diffusion of dopant profiles. Oxidation occurs at room temperature in an inductively coupled RF oxygen plasma. Results from MBE wafers showed oxide breakdown voltages of 8-9 $MVcm^{-1}$, which was very similar to results obtained on substrate material [*Taylor 1991*].

Another problem area concerns device isolation. The production of a δ-FET device is complicated by having the active conducting channel buried below the silicon surface. A conventional MOS process uses a thick field oxide and a channel stop implant to prevent the formation of a parasitic transistor. For the δ-FETs, trench isolation of the device, combined with oxidation of the trench side walls for passivation was used.

The previous use of a rapid thermal anneal (RTA) to activate implanted contacts on MBE devices had shown that an anneal at 1000°C for 30seconds was sufficient for activation. To reduce possible broadening of the delta layer, a shorter anneal of 1000°C for 5seconds was used. This would give at least 90% activation of the implants whilst reducing the thermal budget for each layer [*Gundlach 1991*].

The normal self aligned gate process typically used in MOS fabrication uses a polysilicon gate to define the source/drain contact areas. This appears to have several disadvantages. First the polysilicon is deposited at temperatures >575°C [*Sze VLSI 1988*]. Doping of the gate via an implant and subsequent activation anneal may exceed the thermal budget allowed. Also the implant would need to very carefully tailored such that it does not penetrate through the gate oxide.

3.9.2 DELTA-FET FABRICATION PROCESS SEQUENCE

Six boron delta doped wafers with a range of layer depths and concentrations (table 3.5), and one n-type substrate, used as a control, were processed by the Edinburgh Microfabrication Facility into FET devices. A metal gate processing schedule was used, utilising mask set Eu842 [University of Warwick mask]. A schematic of the δFET is shown in figure 3.19. In total three different gate area FETs were produced $20x100\mu m^2$, $20x20\mu m^2$, and $5x100\mu m^2$ (lengthxwidth).

A schematic of the processing steps is given in figure 3.20 (photolithography stages are assumed). Mask 1 defined the mesa structure of the FET device. Pyrolytic oxide, deposited at 430°C was used as a mask for 0.2μm reactive ion etch. Mask 2 defined the source and drain contact areas, which were formed by ion implantation of $1x10^{15}cm^{-2}$ BF_2^+ at 40keV. The distance between the contacts defining the gate length. All wafers were then given a standard RCA clean to remove carbon contamination of the silicon surface before plasma oxidation. This consumed 22.5nm of silicon to produce 50nm of gate oxide, which also served to passivate the surface. Mask 3 defined the source and drain contact windows. A furnace rapid thermal anneal(RTA) was used for implant activation. Each wafer being individually annealed at 1000°C for 5 seconds. A polyimide coat (5 minutes at 450°C) was then used to planarise the surface. This stage enabled the gate metal to bridge the trench between the active mesa structure and the gate bonding pad. Using mask 4, the source/drain and gate windows were defined on the polyimide field. This was removed by another reactive ion etch. Mask 5 defined the metallisation areas with the final process step of the aluminium sinter performed at 435°C for 20mins in an N_2/H_2 atmosphere. The rapid thermal anneal is the only high temperature stage used in processing.

The processed wafers were half sawn into $3x3mm^2$ chips, with alternate rows and columns left blank for further characterisation. Device characteristics were obtained from an HP4145B semiconductor parameter analyser, with the wafers mounted on a Wentworth MP1000W probing station. All precautions against static

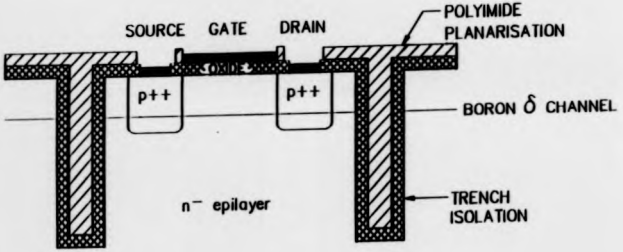
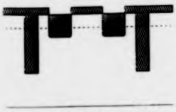


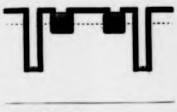
Figure 3.19 Schematic of δFET.

(a) Pyrolytic oxide deposition (@ 430°C).

(d) Oxide strip.



(g) Contact implantation
(BF_2 $1x10^{15}$ atoms cm^{-2} @ 40keV).

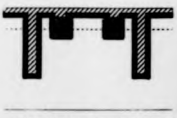


(j) Oxide etch.

(b) Oxide reactive ion etch (RIE).

(e) Pyrolytic deposition.

(h) Oxide strip.

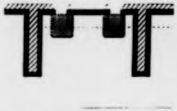


(k) Rapid thermal anneal (1000° 5s),
Polyimide coat and cure.

(c) Trench RIE etch.

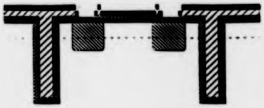
(f) Oxide RIE etch.

(i) Low temperature plasma oxidation.



(l) RIE for contact windows and gate exposure

Figure 3.20 Summary of processing step used in the fabrication of the delta doped FET.



(m) Al metallisation.

(n) Al anneal (435°C 20 minutes).

were taken. All measured devices were labelled, to obtain a statistical distribution and each characteristic was plotted and the data recorded onto floppy disc. Extraction of the data to calculate transconductances was via the IEEE bus.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 DOPING SUPERLATTICES

Boron and antimony doping superlattices were investigated for enhanced carrier mobility by measurement of the temperature dependent Hall mobility. Sample preparation for the Si:B DSL is described in chapter 3.7.3. The difficulty in making suitable contacts on these structures lead to the use of microfabricated Hall structures for the study of the Si:Sb DSL's.

Compositional analysis was by Secondary Ion Mass Spectrometry(SIMS) and the depth dependent carrier concentration was investigated by electrochemical capacitance voltage profiles(e-CV).

4.1.1 Si:B DOPING SUPERLATTICES

Confirmation of a superlattice structure was provided by e-CV and SIMS profiles. {SIMS analysis carried out for the author by SIMS analysis group, University of Warwick 1988. Analysis conditions of a normal incident O_2^+ primary ion beam at 4keV were used}. Figures 4.1 and 4.2 show the SIMS and e-CV profiles obtained on layer 116.7, and the similarity indicates complete electrical activation. These profiles suggest that the dynamic range is limited to 10:1, as opposed to the value of 1000:1, which would be expected given the residual doping level of $10^{16}cm^{-3}$. Also observed are that the amplitude of the oscillations is seen to decay with increasing depth. This effect

could be associated with uneven etching of the crater [*McPhail et al* 1988]. Annealing studies of this sample by McPhail indicated that at 760°C for 32minutes was sufficient to "erase" the perodicity. It is believed then that the dynamic range is limited by diffusion effects associated with the comparatively high growth temperature of 760°C. An alternative explanation for the observed profile is that diffusion has occurred on the first few peaks grown. The e-CV shows evidence for this effect, even though the profile may be smeared due to uneven crater etching. More recent work on boron doping of silicon [*Parry et al* 1991] suggests that a lower growth temperature of 450°C would give full activation of the dopant and reduce profile diffusion. The e-CV profile of 68.7(30/30nm) (figure 4.2) represents the limit of depth profiling of a DSL using this technique. This is due to the limitation of the Debye length, which represents the length scale over which the carriers are distributed at an abrupt junction. Thus for p-type silicon doped at $10^{17}cm^{-3}$, L_D is 13nm. The space charge falls to zero over a length of $5L_D$ and the expression for the parallel plate capacitor is not strictly valid. Therefore it is probable that changes in n(x) may not be resolved in such a DSL. Further e-CV profiles given in figure 4.3a,and 4.4a are shown for layers 68.10 and 68.9. Comparison with SIMS profiles in figures 4.3b and4.4b {SIMS analysis performed for author by Loughborough Consultants Ltd, Loughborough, using O_2^+ primary ion beam at 10keV } shows broad agreement between the profiles. Varying the e-CV etch step to 2nm, from the 4nm typically used for the Si:B DSLs, increased the number of data points per period. However, no increase in the resolution of the peak/valley ratio was found.

The initial Hall mobility results presented here are to verify whether enhanced mobility effects may be observed in a doping superlattice [*Biswas et al* 1988]. Temperature dependent Hall mobility results of a structure(116.7, 30/30nm) with a very similar design to that used by Nakagawa *et al*(1986), are presented in figure 4.5. For comparison, measurements are also given for a homogeneously doped layer of approximately same carrier concentration at room temperature($5x10^{18}cm^{-3}$). The $\mu(T)$ behaviour is typical of phonon scattering at high temperatures(>200K) and ionised

impurity scattering for temperatures < 200K. The DSL shows only a small mobility enhancement, when compared to Nakagawa's result. This may be because of the smearing of the dopant spikes in the present case due to the high growth temperatures used. It should be noted that Nakagawa provided no compositional analysis of the superlattice structures.

The carrier concentration of the authors sample changes from $6.5x10^{18}cm^{-3}$ at 300K to $4.4x10^{18}cm^{-3}$ at 77K. In contrast to this Nakagawa's DSL shows significant freeze out from $5x10^{18}cm^{-3}$ at 300K to $2.5x10^{17}cm^{-3}$ at 77K. For carrier concentrations above $5x10^{18}cm^{-3}$, Si:B has a Mott metal insulator transition [*Kubiak et al* 1987], thus it is reasonable to expect little carrier freeze out for doping levels above this value, and Nakagawa's result must be regarded as suspect. The author is of the view that Nakagawa's results of an anomalous high mobility are in error due to parallel conduction in the substrate.

TABLE 4.1

SUMMARY OF HALL RESULTS OBTAINED FROM AUTHORS AND NAKAGAWA'S MEASUREMENTS

Sample ID.	Carrier Conc. 300K (cm^{-3})	Carrier Conc. 77K (cm^{-3})	Hall mobility 300K ($cm^2V^{-1}s^{-1}$)	Hall Mobility 77K ($cm^2V^{-1}s^{-1}$)
116.7(30/30nm)	$6.5x10^{18}cm^{-3}$	$4.4x10^{18}cm^{-3}$	108	53
Homogeneously boron doped layer	$5x10^{18}cm^{-3}$	$5.3x10^{18}cm^{-3}$	78	45
Nakagawa p-i-p-i DSL	$5x10^{18}cm^{-3}$	$2.5x10^{17}cm^{-3}$	1000	20000

The present results obtained may be interpreted using the two layer expressions for the Hall coefficient given in chapter 2.5. If a structure is composed of equal width doping spikes and where n_2 is the areal concentration of a low doped layer with mobility μ_2, and n_1 is the areal concentration of the heavily doped layer with mobility μ_1, the measured mobility μ from equation 2.25:

$$\mu = \frac{n_1\mu_1^2 + n_2\mu_2^2}{n_1\mu_1 + n_2\mu_2} \qquad (4.1)$$

Then if $n_1 = 10n_2$ and $\mu_2 = 3\mu_1$, the mobility from equation 4.1 is $\mu = 0.48\mu_2$. In such a situation the measured mobility is dominated by the highest mobility carriers in the low doped regions. Charge carrier spillage will further increase the number of carriers in the low doped regions where there will be less ionised impurity scattering.

4.1.2 Si:Sb DOPING SUPERLATTICES

The doping superlattices in this study were designed in light of the previous work on the Si:B DSL's. To produce a systematic study, a range of structures were grown where the doping density in the high doped regions("mark") was kept constant and the width of the nominally undoped spacer("space") was varied between 3 and 40nm (table 3.2).

Growth of all the layers was on 0.4μm buffer nominally doped at $1x10^{16}cm^{-3}$ p-type to act as an extension of the p- substrate. Hence impurities at the epi/substrate interface would not contribute to the electrical conduction. All the layers were processed into Greek cross Hall structures using the Edinburgh Microfabrication facility. Multiple phosphorus implants of $5x10^{15}cm^{-2}$ at 180keV and $1x10^{15}cm^{-2}$ at 40keV allowed at least 0.5μm of the epitaxial layer to be contacted.

Compositional analysis of one of the Si:Sb DSL's was by SIMS carried out for the author by Cascade Scientific Ltd. Analysis conditions on 112.14(3/20nm) DSL, consisted of an O_2^+ primary ion beam at 2keV at the sample, with an electronic gate to maximise the depth resolution. The profile is shown in figure 4.6 and confirms the correct growth of the structure. The width of the dopant spikes is dependent on ion beam mixing effects while the reduction in the amplitude of the structure with depth is due to uneven etching of the craters.

Hall mobility versus temperature results from the Si:Sb DSL's are presented in figure 4.7, with a summary of the results at 300 and 77K given in table 4.2.

The rapid fall in mobility for temperature less than 20K is identified with freezing out of conduction in the low doped regions, leaving low mobility carriers in the doping spikes which possibly move by hopping conduction in an impurity band.

The variation in mobility of the Si:Sb DSL's with 3D concentration at 300K and 77K is shown in figures 4.8 and 4.9 respectively. It is seen that the conductivity increases with the space/mark ratio. These effects are tentatively ascribed to charge carrier spillage from the high doped regions into the low doped regions, where these carriers experience less ionised impurity scattering. Comparison of the highest mobility structure 112.10(30/400nm) where the mobility is $2211 cm^2V^{-1}s^{-1}$ at 77K, with uniformly doped material of the same 3D carrier concentration at 77K, [*Kubiak et al* 1987] shows an apparent mobility enhancement of two.

It has been demonstrated that a high low DSL can have increased an increased mobility as compared to homogeneously doped material of the same 3D carrier density and may be of use in device applications.

TABLE 4.2

SUMMARY OF HALL COEFFICIENT RESULTS ON Si:Sb DSL's

Sample ID.	space/Mark ratio	Overall Thickness (μm)	Carrier Conc. 300K (cm^{-3})	Carrier Conc. 77K (cm^{-3})	Hall Mobility 300K ($cm^2V^{-1}s^{-1}$)	Hall Mobility 77K ($cm^2V^{-1}s^{-1}$)
113.16	1	0.183	$4.8(\pm0.1)\times10^{17}$	$8.2(\pm0.1)\times10^{16}$	446(±5)	560(±5)
112.12	3.33	0.393	$5.6(\pm0.1)\times10^{17}$	$1.1(\pm0.1)\times10^{17}$	429(±5)	516(±5)
112.14	6.67	0.720	$3.2(\pm0.1)\times10^{17}$	$5.1(\pm0.1)\times10^{16}$	558(±5)	1033(±10)
112.10	13.33	1.023	$2.0(\pm0.1)\times10^{17}$	$2.9(\pm0.1)\times10^{16}$	689(±5)	2211(±15)

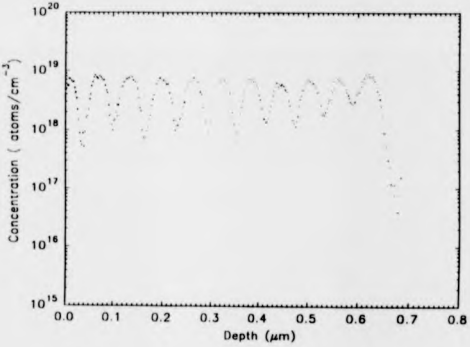


Figure 4.1 SIMS profile of 10 period boron doping superlattice (68.7).

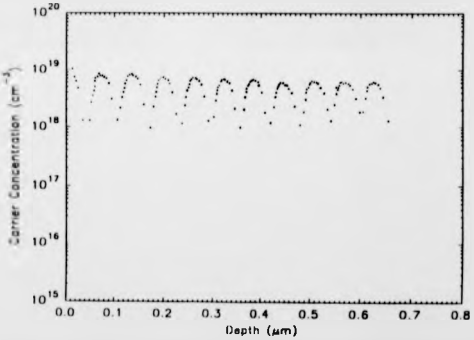


Figure 4.2 Electrochemical CV profile of 10 period boron doping superlattice (68.7).

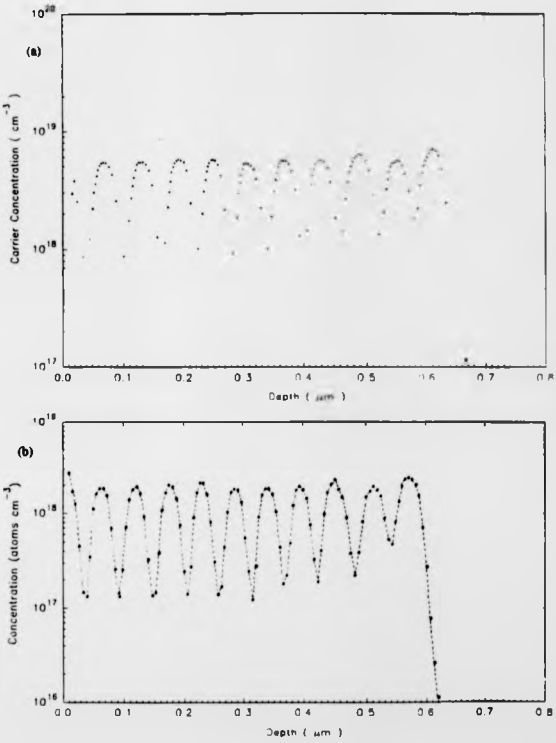


Figure 4.3 (a) Electrochemical CV profile of 68.10(30/60nm) Si:B DSL, (b) SIMS profile of same structure.

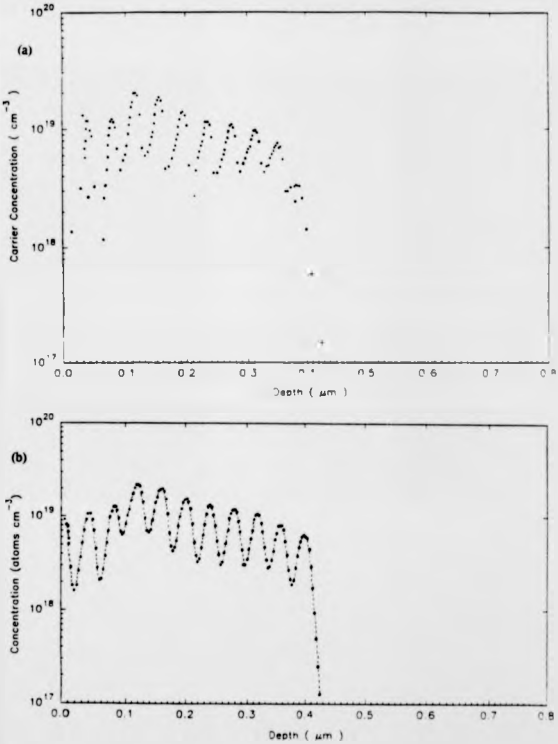


Figure 4.4 **(a) Electrochemical CV profile of 68.9(30/15nm) Si:B DSL, (b) SIMS profile of the same structure.**

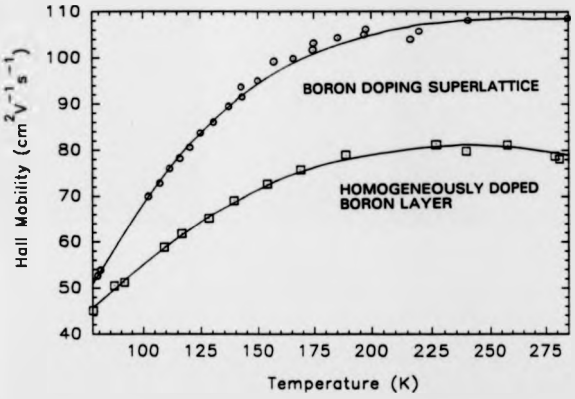


Figure 4.5 Hall mobility vs temperature variation for 68.7(30/30nm) boron DSL, and a homogeneously doped layer of equivalent carrier concentration.

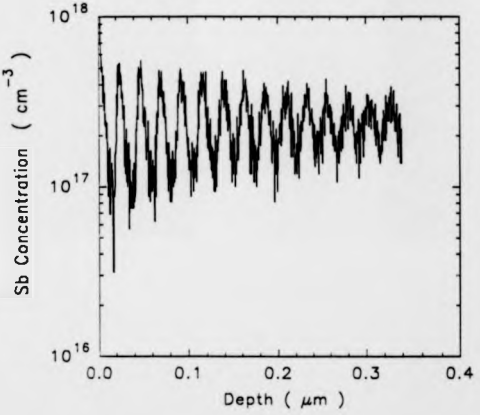


Figure 4.6 SIMS profile of 3/20nm period Si:Sb DSL. {Profiling conditions of an O_2^+ primary ion beam at 2keV at the sample}

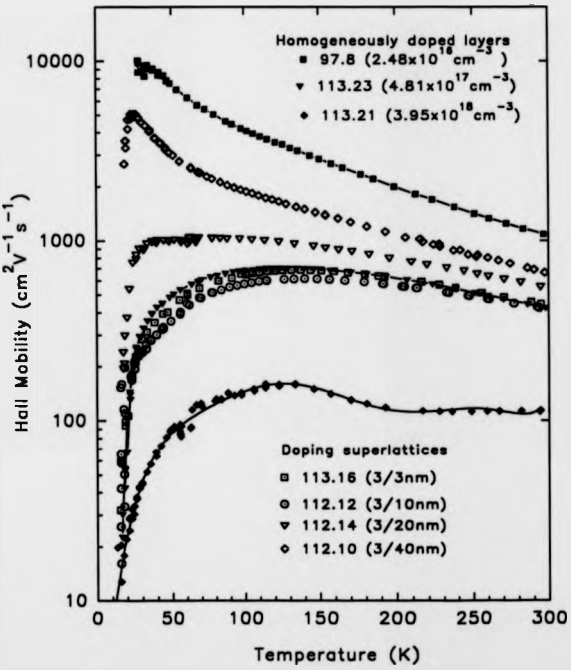


Figure 4.7 Hall mobilities vs temperature variation for Si:Sb DSL and homogeneously Sb doped material.

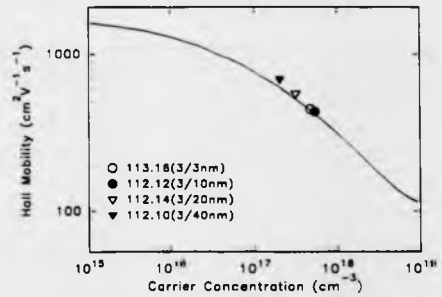


Figure 4.8 Comparison of Si:Sb DSL with homogeneously Sb doped material at 300K. Solid curve obtained from Kubiak *et al* 1987.

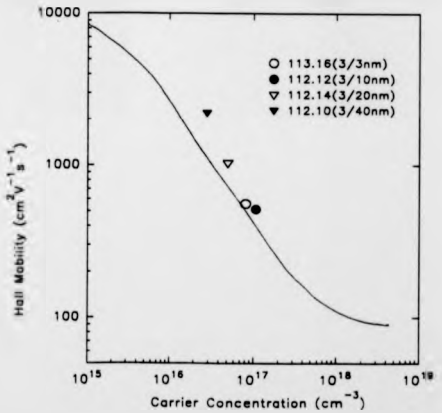


Figure 4.9 Comparison of Si:Sb DSL's with homogeneously Sb doped material at 77K. Solid curve obtained from Kubiak *et al* 1987

4.2 TUNNELLING SPECTROSCOPY OF Si:B AND Si:Sb DELTA LAYERS

The quantum confinement effects associated with delta doping has been investigated via tunnelling spectroscopy. The 2D subband structure produces a staircase density of states, that is observable as discontinuities in the current voltage characteristics. Si:B and Si:Sb delta layers were investigated, and the resulting spectra compared with theoretical modelling of the subband energies. Measurements were carried out at 4.2K, using the experimental measurement procedure described in chapter 3.6, with the sample preparation described in chapter 3.7. Hall and SIMS characterisation confirmed the sheet concentration, width and depth of the delta layers.

4.2.1 SIMS AND HALL CHARACTERISATION OF TUNNELLING SPECTROSCOPY DELTA LAYERS

Secondary ion spectrometry analysis of the tunnelling spectroscopy layers 116.15(Si:B) and 8.31(Si:Sb) was carried out for the author by the University of Warwick SIMS analysis group. Analysis conditions of a 4keV O^+_2 primary ion beam at normal incidence was used on the Si:B delta layer (figure 4.10). The areal density as deduced by the SIMS was $2.3(\pm0.3)\times10^{13}cm^{-2}$ and compares well with a Hall concentration of $2.5(\pm0.2)\times10^{13}cm^{-2}$ at 300K (figure 4.11b). The FWHM is 5nm, however, this width is primarily due to SIMS ion beam induced mixing effects. A consequence of this, is a sharp leading edge and a less steep trailing edge to the profile. { Further comment on SIMS analysis of delta layers in given in chapter 5 }. Hall results were obtained on a van der Pauw structure using NiCr annealed at 460°C to form the ohmic contacts. The temperature dependent Hall mobility is plotted in figure 4.11a. A mobility of $32(\pm3)cm^2V^{-1}s^{-1}$ at 300K is similar to that measured by Mattey *et al* (1990A), Hakim *et al* 1992, for an equivalent concentration Si:B delta.

The SIMS profile of the Si:Sb layer is given in figure 4.12. The areal density of $2(\pm 0.2)x10^{14}cm^{-2}$ compares well with the Hall carrier concentration of $1x10^{14}cm^{-2}$ (figure 4.13b), where this result was obtained assuming a Hall scattering factor of unity. A Hall mobility of $102(\pm 10)cm^2V^{-1}s^{-1}$ (figure 4.13a) is similar to that obtained by Eisele (1989), for an identical delta concentration.

4.2.2 TUNNELLING SPECTROSCOPY

Tunnelling spectroscopy data from the Si:Sb delta layer is presented in figure 4.14. To highlight the tunnelling spectra, the normalised derivative spectra $G=(dI/dV_g)/(I/V)$ has been plotted. The curve shows a number of distinct features, especially between ±75mV. To identify the peaks, a polygonal model, described in section 2.2, was used to calculate the subband energies for an n-type delta layer in silicon. These calculations are presented in a graph of delta sheet carrier concentration against the calculated subband energy (figure 4.15). Comparison with the calculations of Eisele (1989) and Li *et al* (1990) has been given in table 2.1, where fairly good agreement is found for the two lowest subband energies. The features in G occur at 13meV and 40meV relative to the Fermi level, at positive Schottky biases. These dominating features though do not agree with the theoretical calculations of 40 and 275meV obtained from the polygonal. However, if some broadening of the delta is assumed, then Eisele(1989) showed that the subband energy separation reduces. Using Eisele's calculations and performing some extrapolation an estimate of the subband energies can be made. The peaks are assigned as shown in figure 4.14. In this case, the features at positive bias can be identified as E_o' and E_1. The fact that E_1 appears below E_F in the experimental data, but not in the predictions of the polygonal model is not unexpected, due to the limitations of the calculation (see chapter 2.2). The missing E_o

level is probably masked by the high leakage current through the Schottky barrier, shown in figure 4.14. Further features at negative biases indicate the position of unoccupied subbands. It should be noted that the tunnelling spectroscopy of Si:Sb delta layers by Eisele(1989) and Li *et al* (1990) has only shown very broad agreement between the experimental and theoretical calculations, especially for unoccupied levels.

The normalised derivative tunnelling spectra (dI/dV)/(I/V) for the Si:B delta layer is shown in figure 4.16. The most notable feature is the multiplicity of occupied subbands. Modelling of a Si:B delta layer by Mattey *et al* (1992) using a polygonal model, indicated a large number of occupied subbands for a delta layer of sheet density $3x10^{13}cm^{-2}$. However, use of this model to match the experimental data is difficult, due to the tendency of the model to rapidly decrease the subband energy separation for the higher occupied subbands. More detailed modelling has been performed for the author by O'Neill (1991). Here a finite difference method was used to solve Poissons and Schrodingers equation at 0K. The Fermi energy was then calculated using the measured carrier density, and the staircase density of states function. Screening was included with electrons described by 3D Fermi dirac statistics. Boundary conditions of zero potential at the surface, with the delta layer represented by a 0.5nm layer doped at $6x10^{20}cm^{-3}$ between a 20nm n-type cap of $1x10^{16}cm^{-3}$ and a 400nm n-type cap of $1x10^{16}cm^{-3}$. The method was applied to an electron system and found to agree with the self consistent calculations of Li *et al* (1990). The effective masses used, were obtained from INSPEC(1988) where the heavy hole mass(hh) is $0.4m_o$ a light hole mass(lh) is $0.16m_o$ and a third spin split band(so) by 44mev is $0.24m_o$. The agreement between the observed and calculated subband minima is satisfactory, and is shown by arrows in figure 4.16. The possibility that the peaks on the right hand side represent further minima has not been tested, because of the inaccuracy of calculations at higher hole energies.

In conclusion, the first tunnelling studies of boron delta layers in silicon have been observed in the IV characteristics, and broad agreement has been found between the experimental and theoretical subband positions.

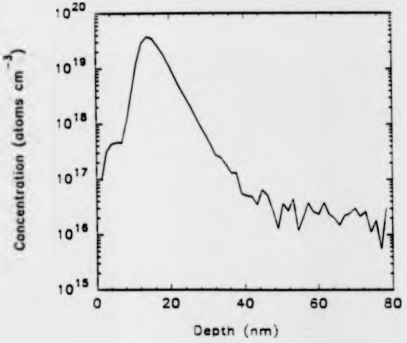


Figure 4.10 SIMS profile of boron delta layer .(116.15) Profile at 4keV O_2^+ at normal incidence. Areal density of $2.3(\pm 0.3)\times 10^{13}cm^{-2}$.

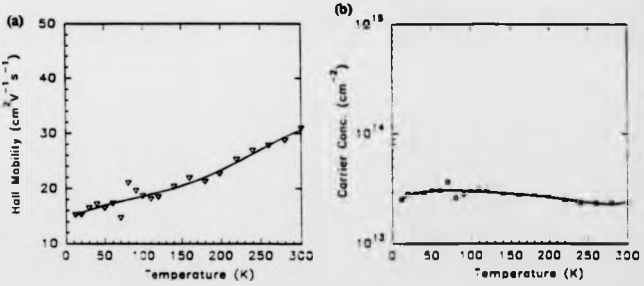


Figure 4.11 (a) Temperature variation of the Hall mobility for a boron delta layer used in tunnelling spectroscopy measurements. (b) Carrier concentration variation with temperature.

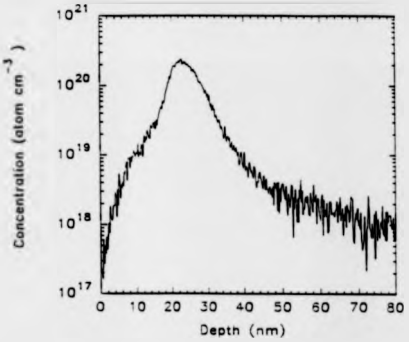


Figure 4.12 SIMS profile of an Antimony delta layer (8.31). Profile at 1keV O_2^+ at normal incidence. Areal density of $2.0(\pm 0.2)\times 10^{14}cm^{-2}$.

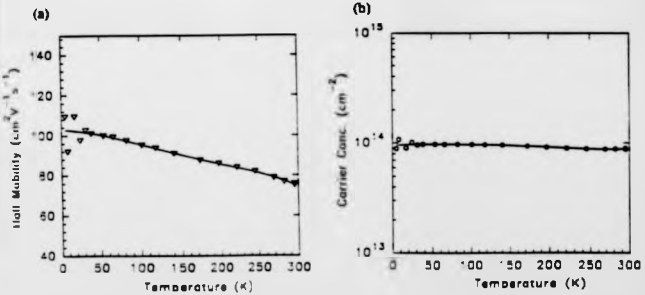


Figure 4.13 (a) Temperature variation of the Hall mobility for the antimony delta layer used in tunnelling spectroscopy measurements. (b) Carrier concentration variation with temperature.

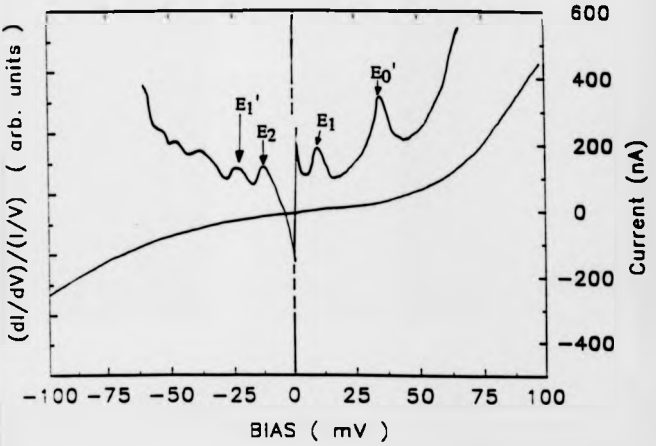


Figure 4.14 Tunnelling spectroscopy curve (dI/dV)/(I/V)obtained from Sb delta layer $2.0(\pm 0.2)\times 10^{14}cm^{-2}$.

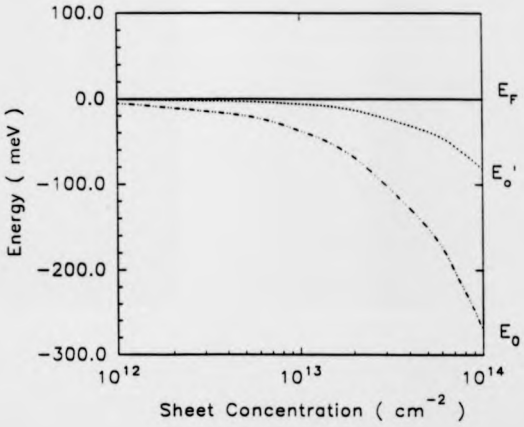


Figure 4.15 Calculated electron subband energies relative to the Fermi level for an n-type delta layer in silicon using a polygonal model.

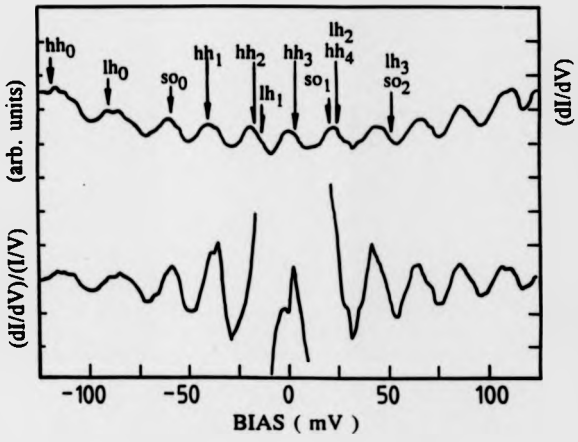


Figure 4.16 Tunnelling spectroscopy curve (dI/dV)/(I/V) obtained from boron delta layer $2.5(\pm 0.3)\times 10^{13}cm^{-2}$.

4.3 WEAK LOCALISATION AND ELECTRON-ELECTRON INTERACTION EFFECTS IN Si:Sb ULTRA THIN DOPING LAYERS

Initial Hall coefficient results in the temperature range 4-300K, on doping layers of widths between 5 and 500nm are shown in figure 4.17. If these results are interpreted in terms of the Mott-Hubbard model of the metal insulator transition [*Mott* 1974], the onset of semiconducting (or insulating behaviour) as the width is decreased would be due to the reduction of coordination number as the dimensionality is reduced[*Mott* 1992]. The 10, 20 and 80nm samples were then used to investigate a 2D to 3D transition in silicon. Detailed measurements were then performed at low temperatures, 0.3K to 25K, and high magnetic fields up to 12T. The corrections to the conductivity due to weak localisation and electron-electron interactions were then compared against current theories.

4.3.1 TEMPERATURE DEPENDENCE OF THE RESISTANCE AND HALL COEFFICIENT

Figure 4.18 shows a plot of the temperature dependent resistivity of the 10nm width layer. The sample resistance is seen to decrease with increasing temperature, and has a logarithmic dependence over the temperature range 0.5 to 10K, which is characteristic of the weak localisation and electron-electron interaction effects discussed in section 2.6. This sample shows similar characteristics to that observed by Bishop *et al* (1980) for a Si MOSFET, whereby the Hall coefficient and resistance saturate at low temperatures. Bishop *et al* (1982) assigned this effect to electron heating effects resulting from the long electron phonon scattering time at low temperatures. The 20nm sample (figure 4.19) similarly shows a logarithmic dependence in the sheet resistance

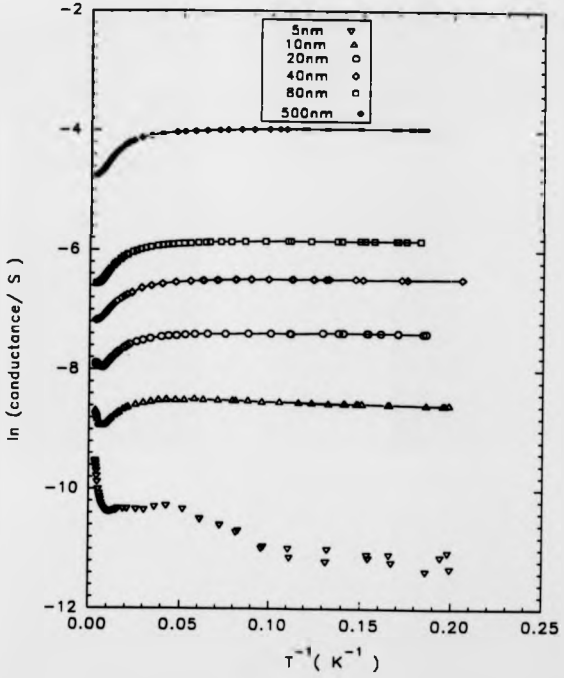


Figure 4.17 Temperature variation (4-300K) of the conductance obtained from Si:Sb doping layers of variable width.

(R) over the temperature range 0.5 to 4K, with a smaller logarithmic dependence in the Hall coefficient (R_H). The 80nm sample, figure 4.19 shows no apparent logarithmic dependence. This can be observed from figures 4.21 and 4.22, which shows the percentage change in R and R_H relative to the values at 1.4K. It appears that the absolute magnitudes of the fractional change in the sheet resistance and Hall coefficient is dependent on the sample width.

According to the theory described in chapter 2.6, the Hall coefficient is sensitive only to interactions. The 2D expression for the correction to the Hall coefficient given by equation 2.33, and may be written as:

$$\frac{\delta R_H}{R_H} \cong -2R\frac{e^2}{2\pi^2\hbar}\left(1-\frac{3}{4}F^*\right)\ln\frac{kT\tau}{\hbar} \qquad (4.2)$$

where F^* is a screening parameter. Equation 4.2 ignores the contribution of the Zeeman spin splitting, as it is small in the fields used to determine the Hall coefficient. Since the resistance is sensitive to both weak localisation and interaction effects (equ. 2.35), the correction to the resistance may be written as:

$$\frac{\delta R}{R} = -R\frac{e^2}{2\pi^2\hbar}\left(1-\frac{3}{4}F^*+g_v\alpha p\right)\ln\frac{kT\tau}{\hbar} \qquad (4.3)$$

where g_v is the valley degeneracy=2 and α is a phenomenological factor depending on the intervalley scattering and where p is the temperature exponent of the phase breaking rate ($1/\tau_\phi \propto T^p$). From figures 4.18 and 4.19, F^* and $g_v\alpha p$ may be extracted. These are presented in table 4.3, where the values of R and R_H used in equations 4.2 & 4.3 have been extracted at 2K. The sheet carrier density has been found from the relation $1/R_H q$.

F^* is found to be approximately equal to 1 in the present data, in agreement with the observations of Burdis and Dean (1988) on MOSFETs. The values are also approximately independent of carrier concentration in agreement with the predictions Fukuyama (1981).

The multisubband occupancy of the layers leads to several problems regarding theoretical analysis, as the expressions derived are strictly for one subband occupation. For a multisubband situation, as discussed by Mattey *et al* (1992a), the corrections to the conductivity are dominated by the lowest occupied state. This was originally discussed by Iwabuchi *et al* (1989) and Kearney *et al* (1988), who showed that the basic scaling of the weak localisation is unchanged, with multiple subband effects confined to changing the prefactor and the diffusion constant. A reasonable approximation is to treat the situation as a single subband, and assume an effective diffusion constant.

TABLE 4.3

EXTRACTED PARAMETERS OBTAINED FROM WEAK LOCALISATION AND ELECTRON-ELECTRON INTERACTION CORRECTIONS TO THE CONDUCTIVITY

	sample width / 10nm	sample width / 20nm	sample width / 80nm
R / Ω	5350(±25)	1344(±2)	334(±1)
R_{sq} / cm^2C^{-1}	67(±5)x10^4	23.7(±0.2)x10^4	7.50(±0.1)x10^4
N_s / cm^{-2}	9.31(±0.7)x10^{12}	2.63(±0.02)x10^{13}	8.32(±0.1)x10^{13}
N_{3D} / cm^{-3}	9.31(±0.7)x10^{18}	1.31(±0.02)x10^{19}	1.04(±0.01)x10^{19}
μ / $cm^2V^{-1}s^{-1}$	125(±10)	176(±2)	224(±4)
F*	1.00	1.00	-
$g_s\alpha p$	0.86	0.81	-
E_0 (ε_F^1 / meV)	21.7	22.7	E_F=17.31meV
E_1 (ε_F^2 / meV)	10.4	19.7	using 2D statistics
E_0 (ε_F^3/ meV)	6.2	18.9	E_F=22.25meV
E_2 (ε_F^4 / meV)	-	14.6	using 3D statistics
E_3 (ε_F^5 / meV)	-	7.5	
E_4 (ε_F^6 / meV)	-	4.1	
τ / s	1.4x10^{-14}	2.0x10^{-14}	3.32x10^{-14}
D_0 / m^2s^{-1}	2.6x10^{-4}	4.0x10^{-4}	2.2x10^{-4}
D_1 / m^2s^{-1}	1.2x10^{-4}	3.4x10^{-4}	
$k_s\ell$	0.70	0.97	1.11

For a single subband system the diffusion constant D is related to the conductivity by $\sigma = e^2 N(E_F) D(E_F)$, where $N(E_F)$ is the 2D density of states. For this work, difficulties arise in the determination of the appropriate diffusion constant for a multisubband situation.

In this case the conductivity is given by:

$$\sigma = \sum_i g_v^i \frac{n_i e^2 \tau_i}{m_i^*} \qquad (4.4)$$

where g_v^i is the valley degeneracy, m_i^* is the effective mass, and τ_i is the relaxation time of the ith subband. For a quasi 2D system $n_i = m_i^* \varepsilon_F^i / \pi\hbar^2$, where ε_F^i is the energy difference between the Fermi level and the bottom of the ith subband. This then gives the conductivity as:

$$\sigma = \frac{e^2}{\pi\hbar^2} \sum_i g_v^i \varepsilon_F^i \tau_i \qquad (4.5)$$

It is a reasonable approximation to assume that τ_i are essentially the same for all the subbands, i.e. that:

$$\sigma = \frac{e^2 \tau}{\pi\hbar^2} \sum_i g_v^i \varepsilon_F^i \qquad (4.6)$$

Thus to obtain an estimate of τ, the values of ε_F^i are required. It seems reasonable to use the infinite square potential well as a valid approximation for the shape of the confining potential for a doping layer of finite width. The subband positions were determined by summing occupation density over all the occupied subbands using a method similar to that used in the polygonal model described in chapter 2.2. As a check on the validity of this method, the Fermi level in the extreme case of the 80nm doping spike was calculated at 17.31meV using 2D statistics and multiple subband occupancy.

This compares well to a value of 20.22meV calculated using 3D statistics, where the 3D carrier density (n_{3D}) is related to the Fermi level by:

$$n_{3D} = (g_v/3\pi^2)(2m^*_D E_F/\hbar^2)^{3/2} \qquad (4.7)$$

where g_v is the valley degeneracy of silicon=6, m^*_D is the 3D density of states effective mass=$0.32m_o$, and E_F is the Fermi level. Table 4.3 gives the calculated energy levels for the 10 and 20nm doping spikes. Using the first two subband energies, the diffusion constants were found to be within a factor of 2. The disorder parameter $k_F\ell$ (where k_F= Fermi wave vector and ℓ is the elastic mean free path) can then be obtained from;

$$k_F\ell = k_F(D\tau)^{1/2} = \left(\frac{2m^*\varepsilon_F^1}{\hbar^2}\right)^{1/2}\left(\frac{\varepsilon_F^1\tau^2}{m^*_i}\right)^{1/2} = \sqrt{2}\,\frac{\varepsilon_F^1\tau}{\hbar} \qquad (4.8)$$

Calculated values are given in table 4.3, such that $k_F\ell \approx 1$ for both samples. This is close to, but still above the criterion for undergoing a metal-insulator transition. Using 3D statistics the value of $k_F\ell$ for the 80nm is also of order 1. This is to be expected, for samples having approximately the same 3D carrier concentration of $1(\pm 0.4)\times10^{19}cm^{-3}$ and the same background concentration.

The observation of electron-electron interaction effects and weak localisation in 3D samples has accomplished by Long and Pepper for Si:Sb(1984) and by Dai *et al* (1992) for Si:B doped silicon. The 3D correction to the conductivity is given by:

$$\sigma = \sigma(0) + mT^{1/2} + BT^{p/2} \qquad (4.9)$$

where the second term is due to electron-electron interaction effects(section 2.6.1) and the last term is the correction due to localisation effects (2.6.2) [Dai *et al* 1992]. The coefficient p is believed to be 3/2 for a disordered system. Fitting equation 4.9 to the 80nm sample over the temperature range 0.3 to 4K, yields the coefficients given in table 4.4. The magnitude of the coefficient m is in satisfactory agreement with the

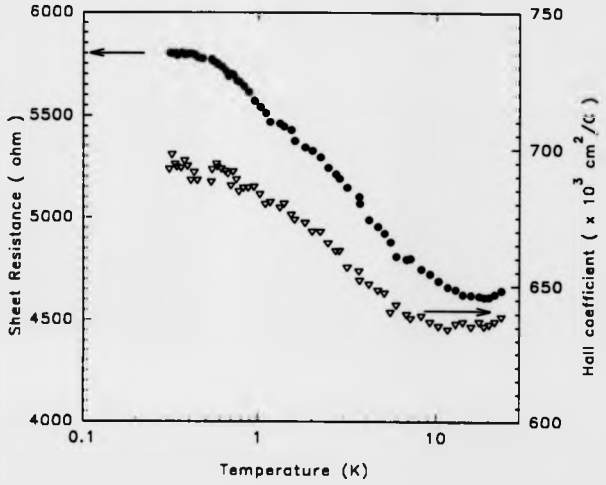


Figure 4.18 Sheet resistance and Hall coefficient plotted against temperature in the range 0.3K to 25K for the 10nm Si:Sb doping layer.

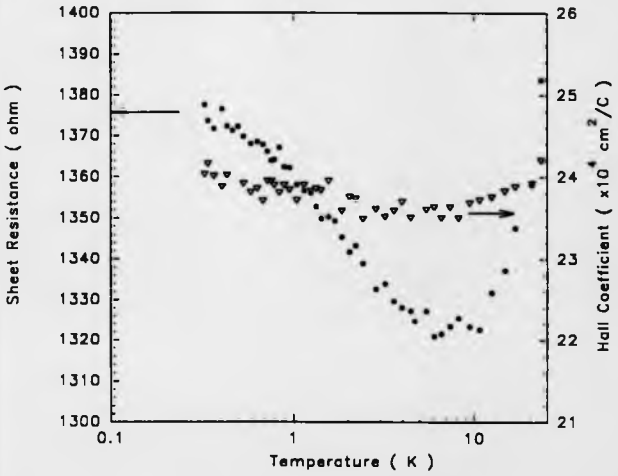


Figure 4.19 Sheet resistance and Hall coefficient plotted against temperature in the range 0.3K to 25K for the 20nm Si:Sb doping layer.

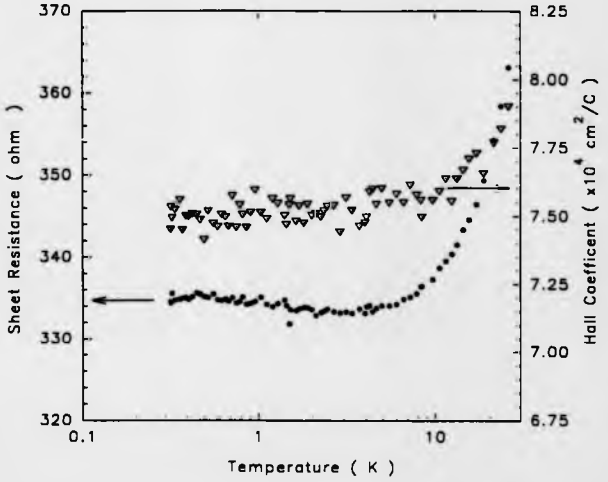


Figure 4.20 Sheet resistance and Hall coefficient plotted against temperature in the range 0.3K to 25K for the 80nm Si:Sb doping layer.

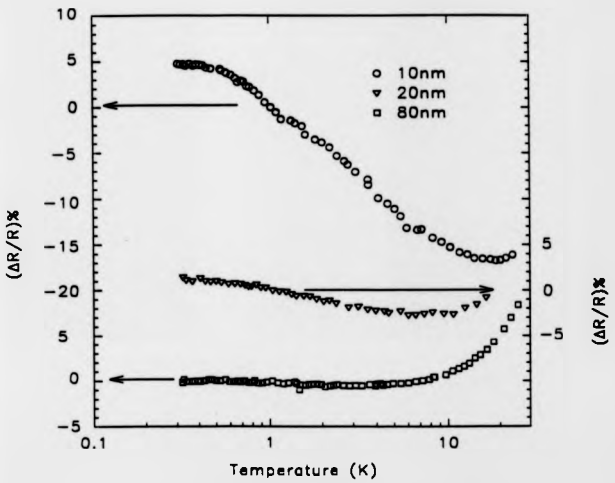


Figure 4.21 Percentage change in sheet resistance for 10, 20, 80nm Si:Sb doping layers relative to the values at 1.4K.

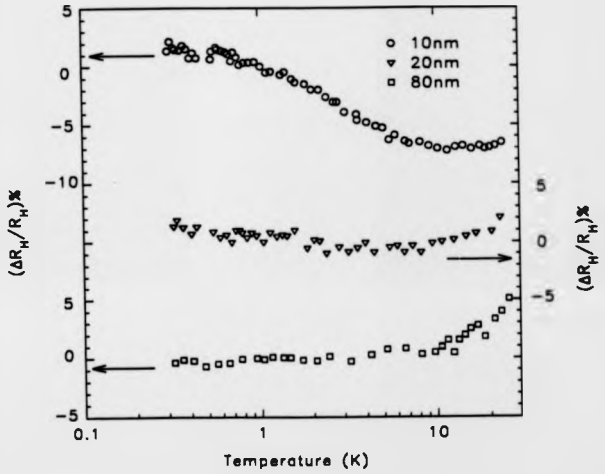


Figure 4.22 Percentage change of the Hall coefficient for the 10,20, 80nm Si:Sb doping layers relative to the values at 1.4K.

values of Long and Pepper(1984). The magnitude of B is also in fairly good agreement with the values of Dai *et al* 1992.

TABLE 4.4

EXTRACTED PARAMETERS FROM 3D W.L AND E-E CORRECTIONS TO THE CONDUCTIVITY

Width w(nm)	p	m ($\Omega^{-1}cm^{-1}K^{-1/2}$) Interactions	B ($\Omega^{-1}cm^{-1}K^{-3/4}$) Localisation
80	3/2	-8 (±2)	6.8(±1.0)

An independent verification of the interaction coefficient could be obtained from the temperature dependent Hall coefficient, using the relation:

$$\frac{\delta R_H}{R_H} = -\frac{2mT^{1/2}}{\sigma(0)} \qquad (4.10)$$

However, extraction of m using this method proved impossible due to the scatter in $R_H(T)$.

4.3.2 MAGNETORESISTANCE STUDIES

The magnetoresistance of the 10, 20 and 80nm samples was measured for sample orientations parallel and perpendicular to the magnetic field. The 10 and 80nm samples were studied at temperatures of 1.40(±0.02)K, 2.02(±0.02)K and 4.00(± 0.02)K and for magnetic fields up to 11.96T. The 20nm layer was studied at 2 further temperatures of 0.320K(±0.002)K and 10.00(±0.02)K. The experimental curves are given if figures 4.23,24,25 for the 10, 20 and 80nm samples respectively.

As discussed in section 2.6.3, weak localisation effects depend on the orientation of the conducting channel to the magnetic field. The 2D nature of the 10nm sample is confirmed by the comparative absence of negative magnetoresistance for sample orientations parallel to the magnetic field.

For a perpendicular field, negative magnetoresistance due to the quenching of the quantum interference is observed. Rewriting equation 2.37 for $a\tau << 1$, where $a = (4eBD / \hbar)$, gives:

$$\frac{\Delta R}{R} = -R\frac{g_v\alpha e^2}{2\pi^2\hbar}\left[\Psi\left(\frac{1}{2}+\frac{\hbar}{4eBL_\phi^2}\right)+\ln\left(\frac{4eBL_\phi^2}{\hbar}\right)\right] \qquad (4.11)$$

where $\Psi(x)$ is the digamma function(*Abramowitz & Stegun* 1965), B is the magnetic field and L_ϕ is the phase relaxation length and $g_v\alpha$ is a valley degeneracy factor of order unity. Fitting the above expression to the 10nm sample, yields the value of $L_\phi = 34$nm at 1.4K. Other temperature values are given in table 4.5. The thermal diffusion length $L_T = (\hbar D / kT)^{1/2}$, where D is the diffusion constant, is estimated to 40nm at 1.4K. Thus the sample width of 10nm is less than both the phase relaxation length and thermal diffusion length confirming the 2D nature of the sample.

TABLE 4.5

PHASE RELAXATION AND THERMAL DIFFUSION LENGTHS FOR 10nm WIDTH SAMPLE

Temperature / K	L_ϕ / nm	τ_ϕ / s	L_T / nm
1.400	34	9.6×10^{-12}	40
4.000	16	2.1×10^{-12}	22

The extracted parameters suggest that p is of order 1, i.e. that $\tau_\phi \propto T^{-1}$. This is in agreement with the earlier calculated values of $g_v\alpha p$, shown in table 4.3.

For the 80nm sample, the magnetoresistance (figure 4.23) is almost isotropic, indicative of 3D behaviour. This is expected since the sample conduction channel width is now much larger than the values of L_ϕ extracted from the 10nm sample. Kawabata (1980) found that the 3D magnetoresistance is temperature independent and is described by:

$$\frac{\Delta R}{R} = -R\,0.605\,\frac{g_s \alpha e^2 w}{2\pi^2 \hbar L_c} \qquad (4.12)$$

where $L_c = (\hbar/eB)^{1/2}$ is the magnetic cyclotron length and w is the width of the sample. A $B^{1/2}$ behaviour is found at low fields for both parallel and transverse sample orientations for the 1.4K and 2K temperatures in the present work. A plot of the fit at 1.4K is given in figure 4.25.

On the basis of the above estimates for L_ϕ, one would expect the 20nm sample to be close to the critical width governing a crossover from 2D to 3D behaviour. The 20nm sample magnetoresistance plotted in figure 4.24, shows considerable anisotropy between sample orientations for sample temperatures $< 4K$. Modelling of the sample is complicated as there are now three relevant length scales, w, L_ϕ, and L_c, which at 1T are all roughly comparable. The most appropriate formula has been derived by Al'tshuler and Aronov (1981) for a sample of finite width, oriented parallel to the magnetic field, assuming the following conditions $L_c^2 >> L_\phi w$, and $L_\phi > w$ [Newson *et al* 1986], then:

$$\frac{\Delta R}{R} = -R\,\frac{g_s \alpha e^2}{2\pi^2 \hbar} \ln\left(1 + \frac{w^2 L_\phi^2}{3L_c^4}\right) \qquad (4.13)$$

Conditions for use of equation are approximately valid, and the values of L_ϕ extracted, given in table 4.6, appear consistent with the 10nm derived values. A plot of the fit at 1.4K is given in figure 4.26.

TABLE 4.6

VALUES OF L_ϕ EXTRACTED FROM 20nm SAMPLE

Temperature / K	L_ϕ / nm	τ_ϕ / s	L_T / nm
0.320	62.75	9.8×10^{-12}	100
1.40	50.12	6.3×10^{-12}	46.7
2.02	40.8	4.2×10^{-12}	39.1
4.00	29.51	2.2×10^{-12}	27.6

Thus the functional form of the magnetoresistance curves can be satisfactorily modelled according to existing theories, which is perhaps surprising given the low values of $k_F\ell$.

There two further observations that can be made on the magnetoresistance data for fields where the Zeeman interaction term will be dominant, i.e. where $g_L\mu_B B >> kT$(g_L is the Lande' g factor is of order 2 and μ_B is the Bohr magnetron).

(i) Since the Zeeman term is a spin effect, it is observable for B fields parallel to the sample. Using the 10nm parallel magnetoresistance data as an example, there is a large positive magnetoresistance for magnetic fields greater than 6T. This is described in section 2.6.3, and the conductivity correction given by equation 2.38, allows an independent verification of the screening parameter F°. Here G(h) is a complicated function, and has been evaluated by Burdis and Dean (1988) for two limiting values;

$$G(h) = 0.091h^2 \cdots\cdots h << 1$$
$$G(h) = \ln(h / 1.3) \cdots h >> 1$$

Thus, a logarithmic dependence of the magnetoresistance is predicted at high magnetic field which is not observed in the experimental data of the 10nm sample given in figure 4.23. A similar effect was inferred by Burdis and Dean (1988), who suggested that the current theories did not fit for low values of $k_F\ell$.

(ii) The functional form of the 80nm magnetoresistance curves follows the work of Yamanouchi *et al* (1967), who observed negative magnetoresistance, at low magnetic fields, in bulk phosphorus doped silicon of a similar carrier concentration. Similarly a large positive magnetoresistance was observed for higher magnetic fields. A further interesting observation from figure 4.25, is the large anisotropy between the different sample orientations at high B fields. This is somewhat surprising given the 3D nature of the sample, inferred in the previous section. This may relate to the behaviour of electrons at high B fields in the six fold degenerate conduction band of silicon.

This work has shown for the first time a 2D to 3D transition occuring in thin doped Si:Sb layers, at low temperatures. Current theories of weak localisation and electron-electron interactions appear to give sensible results for the screening parameter F^{σ}, and $g_v \alpha p$, even though low values of $k_F \ell$ are found in this work. The magnetoresistance has been analysed using current theories. The 10nm width sample has been analysed using 2D theories and the values of L_ϕ extracted indicate that a 2D to 3D transition occurs at around 20nm. The magnetoresistance of a 20nm width sample has also been analysed, and the value of L_ϕ is in sensible agreement with the value for the 10nm sample. The 80nm sample magnetoresistance is isotropic at low B fields indicative of 3D behaviour.

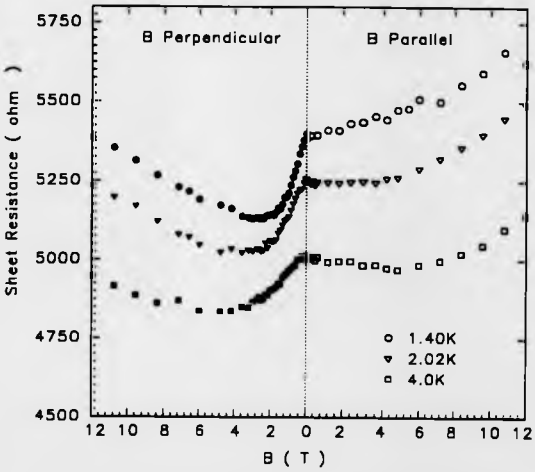


Figure 4.23 Magnetoresistance variation for 10nm sample, at temperatures of 1.4K, 2.02K, and 4.0K.

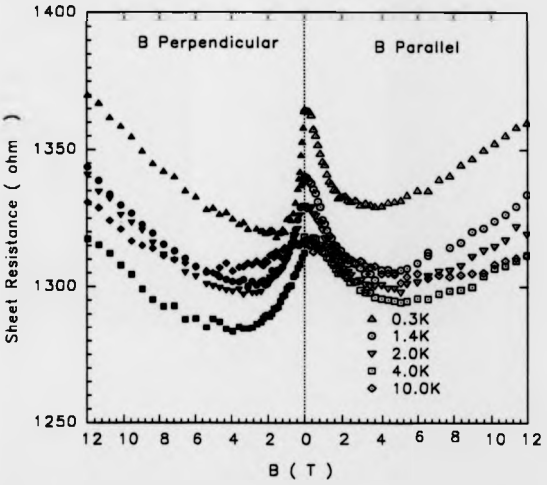


Figure 4.24 Magnetoresistance for 20nm sample, at temperatures of 0.320K, 1.4K, 2.02K, 4.0K, and 10.0K.

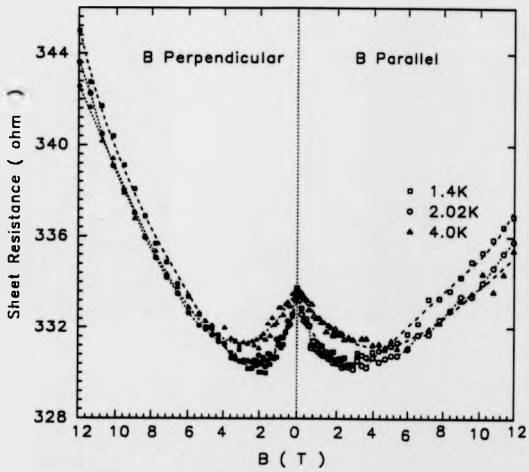


Figure 4.25 Magnetoresistance for 80nm sample, at temperatures of 1.4K, 2.02K, 4.0K. (lines are to guide the reader through the data points).

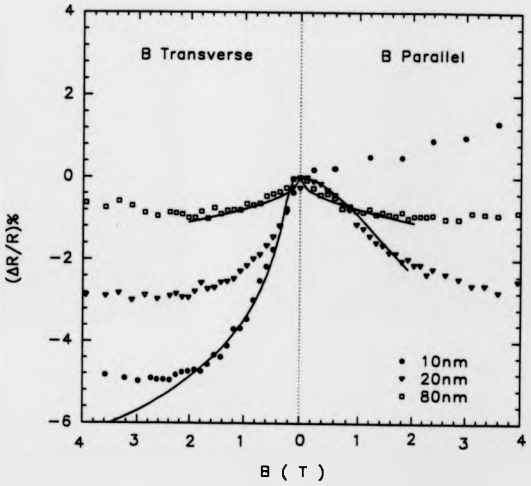


Figure 4.26 Percentage change of the magnetoresistance at 1.4K for 10, 20, 80nm sample. Solid curves are theoretical fits over the appropriate field range.

CHAPTER 5

RESULTS AND DISCUSSION: Si:B DELTA FET

5.1 THE BORON DELTA DOPED FET

Six boron delta doped wafers were processed into δFET devices using the experimental techniques described in chapter 3.9. The wafers were analysed by SIMS to obtain compositional information. Device characteristics from three different gate area δFETs were measured from all wafers. Table 5.1 summarises the intended design specifications and is presented to help in the discussion of the experimental data obtained.

TABLE 5.1

DESIGN SPECIFICATIONS OF PROCESSED δFET WAFERS

Wafer ID.	Nominal Delta Sheet Concentration / cm^{-2}	Nominal Cap thickness /nm
116.7	$1x10^{12}$	20
116.8	$1x10^{12}$	(SIMS control) 42.5
116.9	$5x10^{11}$	20
116.10	$2x10^{12}$	20
116.11	$1x10^{12}$	10
116.12	$1x10^{12}$	30
116.13	$1x10^{12}$	40
116.14	n-substrate used	for PMOS fabrication

5.1.1 COMPOSITIONAL ANALYSIS

Compositional analysis of the boron δ-FET wafers was by secondary ion mass spectrometry (SIMS) carried out under the instigation of the author at Cascade Scientific Ltd, Middlesex. Analysis conditions of a 7.5keV O_2^+ primary ion beam, with an angle of incidence to the surface normal of 52° to give an approximate net ion energy of 3keV at the surface. The samples were cleaned with a 10% HF dip followed by a DI water rinse, to remove the low temperature oxide on the "blank" material. {Note: Not all of a wafer was processed during fabrication. The die size of $3x3mm^2$ allows unprocessed material to be left between processed die's for material analysis. The blank squares have the identical heat and oxidation treatments as a processed chip}

It should be noted that the interpretation of delta profiles for small cap thicknesses is complex [*Barlow et al* 1992], however, given this reservation some observations can be made.

Figure 5.1 shows the profiles of the δ-FET wafers (116.10, 116.7, 116.9) with a fixed layer depth (nominal 20nm), but varying delta sheet density { refer to table 5.1 for design specifications of δ-FET wafers under investigation in this work }. The delta layer in 116.7 shows a much less steep trailing edge to the profile indicating that this delta layer has diffused more than those in wafers 116.10 and 116.9. The nominal delta layer peaks should occur 20nm beneath the surface, but the experimental data indicates a cap thickness of 10nm. However, profiles obtained in this region are not easily interpretable. This is due, for example to a large ion yield change during the pre-equilibrium region [*Barlow et al* 1992].

SIMS profiles for the δ wafers with a nominal fixed layer dose of $1x10^{12}cm^{-2}$ but varying cap thicknesses (116.7,13,12,11) are presented in figure 5.2. Again, the delta layer in 116.7 shows more diffusion compared to the other layers in figure 5.2. Sample 116.11 appears to be extremely close to the surface so that there is no apparent leading edge to the profile. The expected cap thickness of 10nm after oxidation

compared to the SIMS measurement of < 5nm, indicates that the oxidation process to produce the gate dielectric may have consumed more silicon than was anticipated. Measurement of the oxide thickness for 116.12 and 116.11 gave 65±3nm and 52±2nm respectively {Measured for the author by the E.M.F}, against a design specification of 50nm. The extra silicon consumed in producing the thicker oxide would leave the delta layer located 23nm beneath the silicon surface for wafer 116.12. The larger than expected oxide thickness, still leaves the delta layers of 116.12 and 116.13 with distinct profiles, where the measured cap thickness from the SIMS profiles are approximately 10 and 20nm respectively.

To obtain further information on the diffusion of the delta layers during processing, a SIMS profile was obtained on the control layer 116.8 (this sample was unprocessed and received no heat treatment) {figure 5.3}, to compare with an identical specification wafer 116.7 which had been processed into devices. Two parts of wafer 116.7 were profiled, (i) a section from the edge of the layer which had **not been oxidised** {sample ID **116.7(un-ox)** but had undergone all the thermal treatments of processing including the RTA and, (ii) a section of the layer that **had been oxidised {116.7ox}.**

Integration of the peak density(116.8) gives an areal density of $7x10^{11}cm^{-2}$ compared to an as grown specification of $1x10^{12}cm^{-2}$, with the peak correctly located at a depth of 40nm. The full width at half maximum (FWHM) is 7nm, which is expected given the relatively high primary ion energy. For 116.7 (un-ox) the FWHM is now approximately 19nm, with the peak height reduced to a value of $3x10^{17}cm^{-3}$. The profile from 116.7(ox) has a "shifted" origin so that peak heights and widths may easily be compared. The SIMS profile of the delta layer in 116.7 presented in figures 5.1 & 5.2 show that this was a "worst" case example of the diffusion that occurred during processing.

There are though several important observations that can be made from figure 5.3.

(i) The rapid change in the slope of the boron concentration near the surface < 5nm is due to the large ion yield change for boron in SiO_2 as equilibrium during depth profiling is established.

(ii) The trailing slope of the delta layer in 116.8 appears to be the same as the trailing slope for a boron feature located at the silicon surface, which indicates that the surface boron is also sharp feature. This surface boron, whose origin is presently unknown, appears to have been present during processing as the trailing slope features of sample 116.7(unox) are less steep.

The shape of the delta layers as determined from the SIMS profiles is symptomatic with diffusion broadening of a doping spike. The possible causes for this are:

(i) The rapid thermal anneal. The broadening of the delta by some 12nm is unexpected due to the anneal experiment in chapter 3.9.1, results shown in figure 3.18. This suggested that the diffusion broadening was within the SIMS depth calibration measurement. An estimate of the broadening that occurs during the rapid thermal anneal can be calculated from the $\sqrt{Dt}$, where D is the diffusion coefficient and t the time in seconds of the anneal. From the data of Vick(1969), $D = 1 \times 10^{-13} cm^2/s$ at T = 1273K, and with t = 5s used in the R.T.A, then $\sqrt{Dt} = 7nm$. This suggests that a delta layer may broaden by approximately 14nm. Since the rapid thermal anneal was performed manually by inserting wafers one at a time into a furnace, the discrepancies in the widths between the various delta layers can be explained. The RTA stage is the most likely cause of the diffusion.

(ii) It also known that during the oxidation of silicon, there is enhanced boron diffusion, caused by oxygen being injected into the silicon lattice which produces a fast diffusion path for boron through interstitials and vacancies. Experiments by Cowern *et al* 1991 on the thermal oxidation silicon containing a buried boron delta layer confirmed this effect. Whether this problem occurs during plasma oxidation at room temperature requires further investigation.

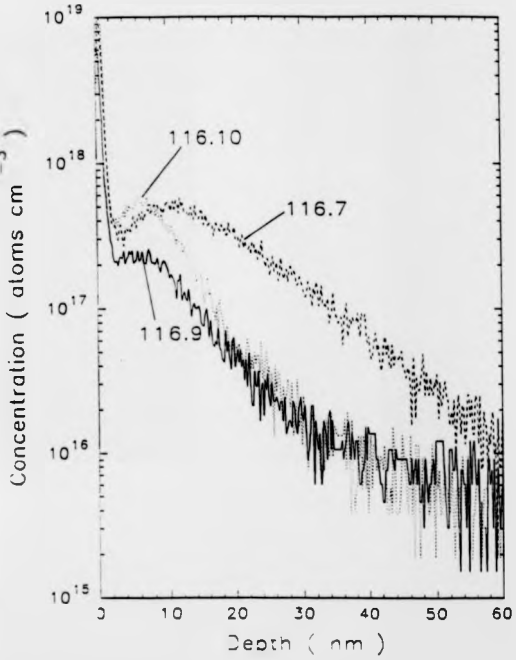


Figure 5.1 SIMS profile of δFET waters 116.10($2x10^{12}cm^{-2}$,20nm), 116.7($1x10^{12}cm^{-2}$, 20nm), 116.9($5x10^{11}cm^{-2}$, 20nm) with fixed layer depth.

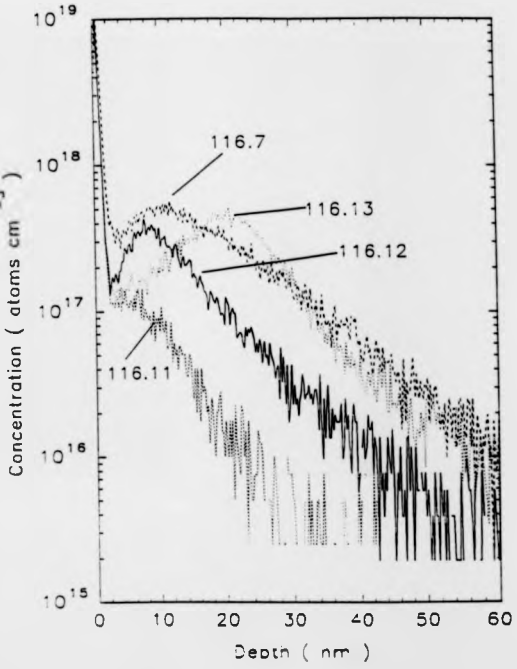


Figure 5.2 SIMS profile of δFET wafers 116.7(1x10^{12}cm^{-2}, 20nm), 116.11(1x10^{12}cm^{-2}, 10nm), 116.12(1x10^{12}cm^{-2}, 30nm), 116.13(1x10^{12}cm^{-2}, 40nm) varying cap thickness and fixed delta layer dose.

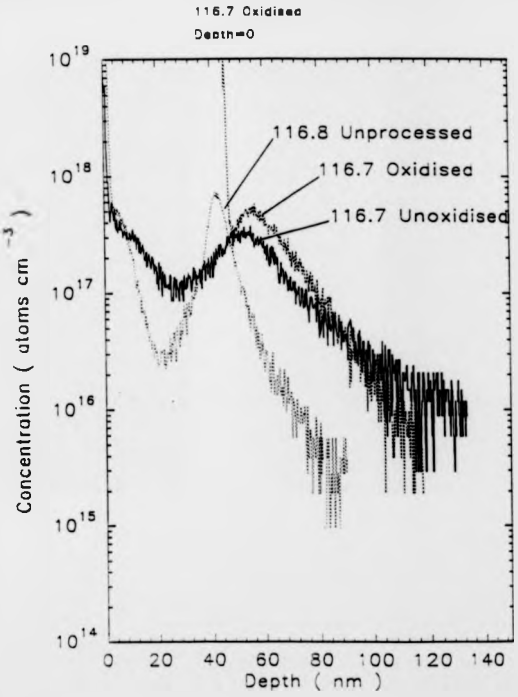


Figure 5.3 SIMS profiles comparing two waters of the same as grown specification 116.8 and 116.7(unoxidised). The profile of 116.7 oxidised is obtained from a blank square in the central portion of the wafer.

The SIMS results indicate that wafers 116.13 and 116.12 have the most distinct delta doping profiles. The measured SIMS FWHM for 116.12,116.13 are approximately 6nm and 15nm respectively. Since the width of the delta layer is less than the silicon cap thickness it is reasonable to assume that the transistor characteristics can be deacribed using the delta FET model presented in chapter 2.7.

5.2 ELECTRICAL ANALYSIS

The source/drain characteristics for the different FET device geometries for wafer 116.12($1x10^{12}cm^{-2}$,30nm) are given in figure 5.4. The $5x100\mu m^2$ device has the largest drain source current as expected for the device with the largest channel width/length ratio from equation 2.48. The features to observe are;

(i) The apparent saturation behaviour of the drain/source curve. This effect was not noticed in the devices of van-Gorkum (1987), although it is predicted by Wood (1991). Nakagawa(1989) showed some saturation in the IV characteristics of the ALD-FET but very little in the Sb-δFET device. The conventional MOSFET of Nakagawa's also showed poor characteristics in comparison, but this may of been due to short channel effects. However, the conventional PMOS FET with the $5x100\mu m^2$ geometry produced in this work suffered no punchthrough.

(ii) The second observed feature is a "kink" at V_{DS}=-15V. This feature remains unexplained.

Figure 5.5 shows a typical characteristics from layer 116.13($1x10^{12}cm^{-2}$,40nm) obtained from a $20x20\mu m^2$ device. The characteristic appears similar to layer 116.12 (figure 5.4). The ratio of the on/off current is > 10 in both of these wafers.

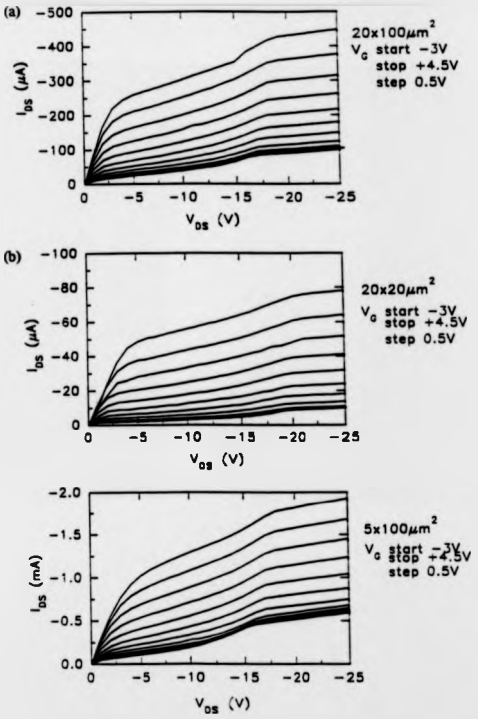


Figure 5.4 IV characteristics of wafer 116.12 (30nm $1x10^{12}$ cm^{-2}). (a) $20x100\mu m^2$, (b) $20x20\mu m^2$, (c) $5x100\mu m^2$ gate area FETs.

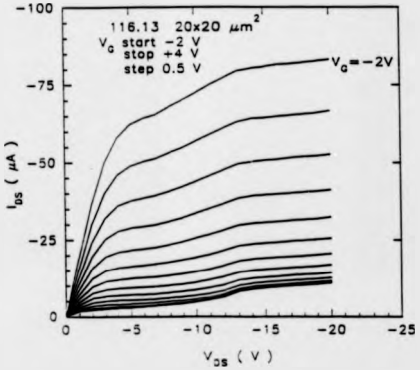


Figure 5.5 Typical saturation drain-source characteristic of a 20x20μm² device from wafer 116.13 (40nm, 1x10¹² cm⁻²).

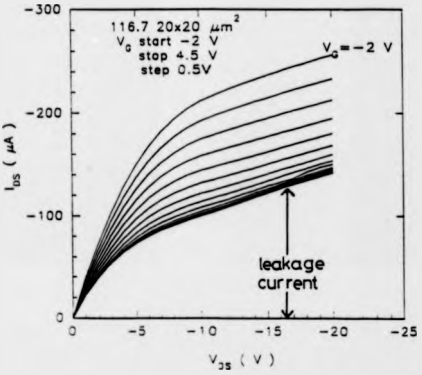


Figure 5.6 Typical saturation drain-source characteristic of a 20x20μm^2 device from wafer 116.7 (20nm, $1x10^{12}$ cm^{-2}). The leakage current is clearly observed.

Figure 5.6 shows a typical characteristics from layer 116.7($1x10^{12}cm^{-2}$,20nm). The most dominating feature is the apparent leakage current at high gate biases. This effect was also found in wafers 116.9,10,11. The ratio of the on/off current for these devices was approximately 2. A post fabrication inspection of mask Eu842, with each mask layer superimposed, showed that it was possible that $20x100\mu m^2$ and $5x100\mu m^2$ devices gate metals may not of covered entire channel area, thus causing a conducting path which is entirely independent of the gate bias. However, there appeared to be no misalignment for the $20x20\mu m^2$ devices, and these devices also exhibited a leakage current in wafers 116.7,9,10,11. The magnitude of the leakage current also appeared to be wafer dependent. No leakage current was found for the PMOS device, but this is expected for a normally off device. Therefore extraction of device parameters such as mobility and transconductance was only obtained from layers 116.12 and 116.13, which showed good switching characteristics.

Using equation 2.45, the pinch-off voltage is proportional to the depth of the delta layer beneath the surface. The extracted pinch-off voltages from the characteristics are $V_p(116.13,40nm)=3.0(\pm0.5)V$ and $V_p(116.12,30nm)=2.0(\pm0.5)V$ respectively.

5.2.1 TRANSCONDUCTANCE AND MOBILITY EXTRACTION

The present author has obtained in chapter 2 an expression relating the transconductance of a δFET to device parameters. Using equation 2.47 the transconductance of a long channel FET device is given as;

$$g_m = N_D \frac{q\mu Wa}{L}\left(1+\frac{V_G}{V_p}\right) \qquad (5.1)$$

where Vp pinch-off voltage($V_p = aqN_D/C$) and μ is the mobility.

Differentiating equation(5.1) with respect to V_G gives:

$$\frac{dg_m}{dV_G} = \frac{\mu WC}{L} \qquad (5.2)$$

where C is the series capacitance per unit area of the oxide+Si:cap (equation 2.41). Thus a plot of g_m vs Vg (figure 5.7) allows determination of the channel mobility from the slope [*Biswas et al* 1992]. Numerous devices have been plotted to obtain an average. The mobility results are summarised in Table 5.2. The capacitance per unit area has been calculated from the nominal device specifications.

TABLE 5.2

EXTRACTED MOBILITIES FROM WAFERS 116.12 AND 116.13

Wafer ID	Nominal δ-layer depth (nm) and Conc. (cm-2)	Device geometry length x width (μm)	Mobility ($cm^2V^{-1}s^{-1}$)
116.12	30, $1x10^{12}$	100x20	80±15
116.12	30, $1x10^{12}$	20x20	74±12
116.12	30, $1x10^{12}$	5x100	54±20
116.13	40, $1x10^{12}$	100x20	78±3
116.13	40, $1x10^{12}$	20x20	68±5
116.13	40, $1x10^{12}$	5x100	53±7

Mask Eu842 used for processing, also contained a Hall bar device structure. However, severe difficulty was found in bonding and measuring the samples, due to the polyimide layer beneath the metal bonding pad. The only consistent results were obtained from wafer 116.13(40nm), where $N_s=5(\pm0.2)x10^{11}cm^{-2}$ and $\mu=145(\pm10)cm^2/Vs$. This concentration is low compared to the intended as grown specification of $1x10^{12}cm^{-2}$. The mobility is consistent with the recent work of Hakim *et al* 1992 who measured the Hall mobilities of boron delta layers. Table 5.3 gives a summary of the Hall data obtained from the delta FET wafers. The Hall data from wafers 116.9 and 116.12 was only obtained from one working Hall device. The lower

mobilities obtained from equation 5.2 are consistent with the reduced mobility due to the field effect. For the 5μm gate length, the field at 10V is $2x10^4$V/cm where the hole velocity is beginning to saturate [*Jacobini et al* 1977].

TABLE 5.3

SUMMARY OF HALL MEASUREMENT OBTAINED FROM δFET WAFERS

Wafer ID	Growth Ns (cm^{-2})	Hall Ns (cm^{-2})	Resistance (ohm squ.)	Hall Mobility ($cm^2V^{-1}s^{-1}$)
116.9	$5x10^{11}$	$1.8x10^{12}$	$2x10^6$	173
116.12	$1x10^{12}$	$4x10^{11}$	$8x10^6$	190
116.13	$1x10^{12}$	$5x10^{11}$	$7.9x10^6$	145

A method (suggested to the present author by Wood (1992)) for determining whether a parasitic channel is operating in the device characteristics, can be obtained from a plot of g_m^2 vs I_D. Using the expression derived in chapter 2 for the source drain current (equation 2.48) and differentiating w.r.t V_G gives:

$$\frac{g_m^2}{I_{DS}} = \frac{2W\mu C}{L} \qquad (5.3)$$

where C is the series capacitance of the silicon and the gate oxide, given by equation 2.41. Equation 5.3 can be similarly obtained from the expression for the source drain current of a conventional MOSFET in the saturation region. Figures 5.8 and 5.9 show a plots of g_m^2 vs I_D for a range $20x20\mu m^2$ devices from wafers 116.13 and 116.12. Clearly observed are two linear regions of operation, with a change in slope of approximately 2 for drain source currents greater than 10-15μA. This change is probably partially due to a change in the capacitance or more likely, largely due to a change in the mobility on the formation of an inversion layer at the SiO_2/Si interface

for negative gate biases. Low source drain currents correspond to the operation of a depletion mode boron δFET, with an operational voltage window between -1 and 3V. From the characteristic associated with delta channel operation, and using equation 5.3, a mobility of $70(\pm5)cm^2V^{-1}s^{-1}$ can be extracted for 116.13 and $64(\pm10)cm^2V^{-1}s^{-1}$ for 116.12 which is similar to the values calculated in table 5.2.

Repeated measurement of devices after a few days showed that gate oxide broke down after the application of a small bias. Stressing of gate oxides is a well known problem, but with the voltages used, this should not of been a problem. A typical breakdown field strength (E_{ov}) of 9MV/cm is obtained for a plasma oxide on substrate [*Taylor* 1992]. For layer 116.10 the gate current was extremely low $< 10pA$ ($< 10^{-7}$ Acm^{-2}), for $V_{DS} < 20V$. Larger voltages though, lead to catastrophic breakdown, with an E_{ov} of $4.5MVcm^{-1}$. This may possibly be related to the defect density of the material.

The yields obtained from the measured devices are given in table 5.4. {A working device was defined as one in which modulation of the source drain characteristic was obtained by a variation in the gate bias.} The higher yields for small gate areas may be due to the lower defect density within the smaller devices. A dislocation density of $\approx 1x10^5cm^{-2}$ for each wafer was found using a dilute Schimmel etch [Phillips 1992]. However a processing related fault also led to a lower yield for the $5x100\mu m^2$ devices due to an overetch of the metal contact strip between bond pad and gate metal.

The successful fabrication of the first p-channel delta doped FET has been shown in this work. A low temperature processing schedule has been used to fabricate the δFET devices. SIMS results indicated that some diffusion broadening of the delta layer has occurred probably during the rapid thermal anneal stage. A model presented in this work describing the operation of a long channel δFET has been used to extract the mobility in the delta channel. Clear evidence for delta channel operation is obtained

by a change in slope from a plot of the square of the transconductance versus the saturation drain-source current.

TABLE 5.4

YIELD OBTAINED FROM BORON δFET DEVICES

Wafer I.D.	$100x20\mu m^2$ % Yield	$20x20\mu m^2$ % Yield	$5x100\mu m^2$ % Yield
116.7	14	32	29
116.9	23	55	45
116.10	0	19	29
116.11	10	24	24
116.12	38	52	62
116.13	33	50	33
116.14	44	66	22

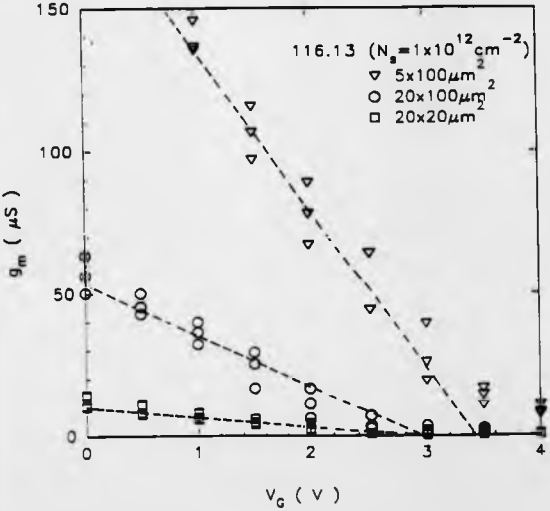


Figure 5.7 Plot of g_m vs V_G for numerous 20x20μm^2 devices from layer 116.13(40nm, 1x10^{12}cm^{-2})

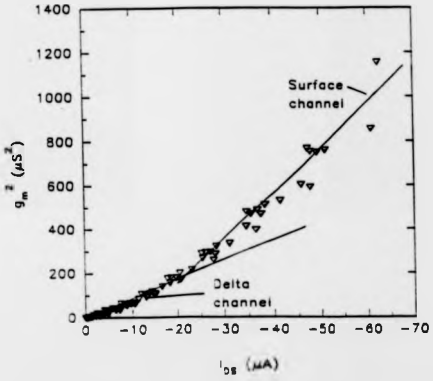


Figure 5.8 Plot of g_m^2 vs I_D for numerous 20x20μm² devices from wafer 116.13(40nm, 1x10¹²cm⁻²).

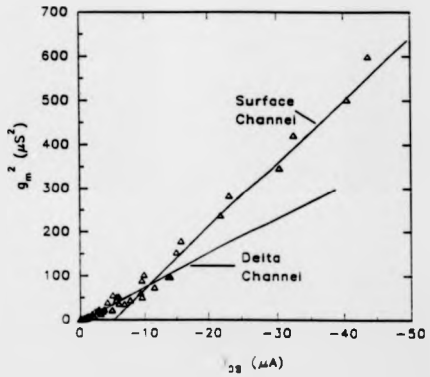


Figure 5.9 Plot of g_m^2 vs I_D for numerous 20x20μm^2 devices from wafer 116.12(30nm, $1x10^{12}cm^{-2}$).

CHAPTER 6

CONCLUSIONS AND FURTHER WORK

In this thesis the electrical transport properties of high resolution doping structures grown by Si:MBE have been studied. The high degree of profile control, can be exploited in the production of new devices such as the delta doped field effect transistor studied in this work. A periodic sequence of high resolution doping spikes, known as a doping superlattice, in which enhanced carrier mobilities were found by Nakagawa *et al* (1987) was further investigated. Thin layer doping (or delta doping) allowed the study of 2-Dimensional phenomena in a silicon system without the presence of an oxide barrier. This was investigated by tunnelling spectroscopy. Increasing the width of the doping layer allowed a 2D-3D transition to be observed in silicon, by magnetoresistance studies.

Temperature dependent Hall coefficient measurements were used to characterise Si:B and Si:Sb doping superlattices. The anomalous high mobility observed by Nakagawa *et al* (1986) in a boron doping superlattice with a period of 60nm, was not observered by the author in a similar structure. Si:Sb doping superlattices designed to have a high mobility showed apparent mobility enhancement with increasing space/mark ratio. This effect was interpreted as being due to increasing carrier spillage into the low doped regions of the superlattice.

Further work on doping superlattices should involve the use delta doping to achieve the Esaki criterion [*Esaki* 1970] of a large potential modulation with a short superlattice period. Delta doping with opposite type spikes should produce a saw-tooth band-edge profile and allow the formation of minibands. This may then be observable

via transport measurement parallel and perpendicular to the superlattice. Such a structure would be very challenging to produce by Si:MBE, as two different growth processes would be used to produce n and p type delta layers.

The 2D subband structure associated with delta doping was investigated via tunnelling spectroscopy. Reported for the first time in this work, are results of tunnelling studies of boron delta layers in silicon. The observed structure was compared to theoretical calculations which gave broad agreement with the experimental results.

A future tunnelling spectroscopy study could investigate the variation of the measured subband energy with delta layer concentration and layer width. This would be easier to achieve with Sb delta layers, due to the fewer number of occupied subbands, giving more easily resolvable spectra. It may then be possible to improve theoretical calculations of subbands energies. Further investigations of the subband spectrum of boron delta layers in silicon is required.

Transport measurements were then continued on a series of Si:Sb doped thin layers, with widths of 10, 20 and 80nm. A metal-insulator transition was observed as the width of the conducting channel was decreased. Also reported for the first time, is a 2D to 3D transition in silicon. Current theories of weak localisation and electron-electron interaction effects have been used to describe the corrections to the conductivity. The layers studied have a large amount of disorder, where the values of $k_F\ell \cong 1$. 2D transport formula have been used to extract values of the screening parameter F^σ and the phase relaxation time is found to vary as T^{-1}. Magnetoresistance studies on a 10nm width Sb doped layer, has shown a large anisotropy between sample orientations parallel and perpendicular to the magnetic field. Values of the phase relaxation length (L_φ) have been extracted from the negative magnetoresistance found for perpendicular sample orientations. The value of L_φ=34nm justifies the use of 2D transport formula. A 20nm width sample was described using formula for a quasi 2D system parallel to the magnetic field. Again, sensible values of the phase relaxation

length were found. In contrast a 80nm width sample could be satisfactorily described using 3D transport formula and the magnetoresistance was found to be temperature independent and isotropic.

The study of weak localisation and electron-electron interaction phenomena effects should be extended to a Si:Sb delta layer. In such a system, the 2D transport formula should apply for magnetic fields up to 40T. Further theoretical work is required to explain the Zeeman spin spitting effects seen in these layers, as the form of the magnetoresistance for high magnetic field cannot be adequately described. A metal-insulator transition may possibly be observed for a suitable sample on the application of a magnetic field.

Lastly, the device applications of delta doping were investigated by the fabrication of the first p-channel delta doped FET using a boron delta layer. A low temperature processing schedule, combined with a plasma enhanced oxide growth process was used to minimise diffusion of the delta layer. A model is presented describing the operation of a long channel delta doped FET. This was used to extract device parameters such as the channel mobility.

The delta doped FET produced in this work has shown that a working device can be fabricated using Si:MBE delta layer. Optimisation of the RTA stages is needed to reduce further dopant diffusion. Adoption of an n^+ polysilicon gate would allow an investigation of submicron devices using a self aligned process to reduce the parasitic capacitances. This processing would then be more typical of that used to produce CMOS devices. The p-channel FET needs to be demonstrated with an n-type punchthrough stopper. Use of two opposite type delta layers, raises the possibility of the production of a CMOS devices. A mask set with diagnostic test structures, such as Hall Bar and an MOS capacitor to determine carrier concentrations, oxide quality and dopant profiles is needed to correlate the extracted transistor parameters.

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